FTICR PRE-AMP SYSTEM

User Manual

Revision 3.0

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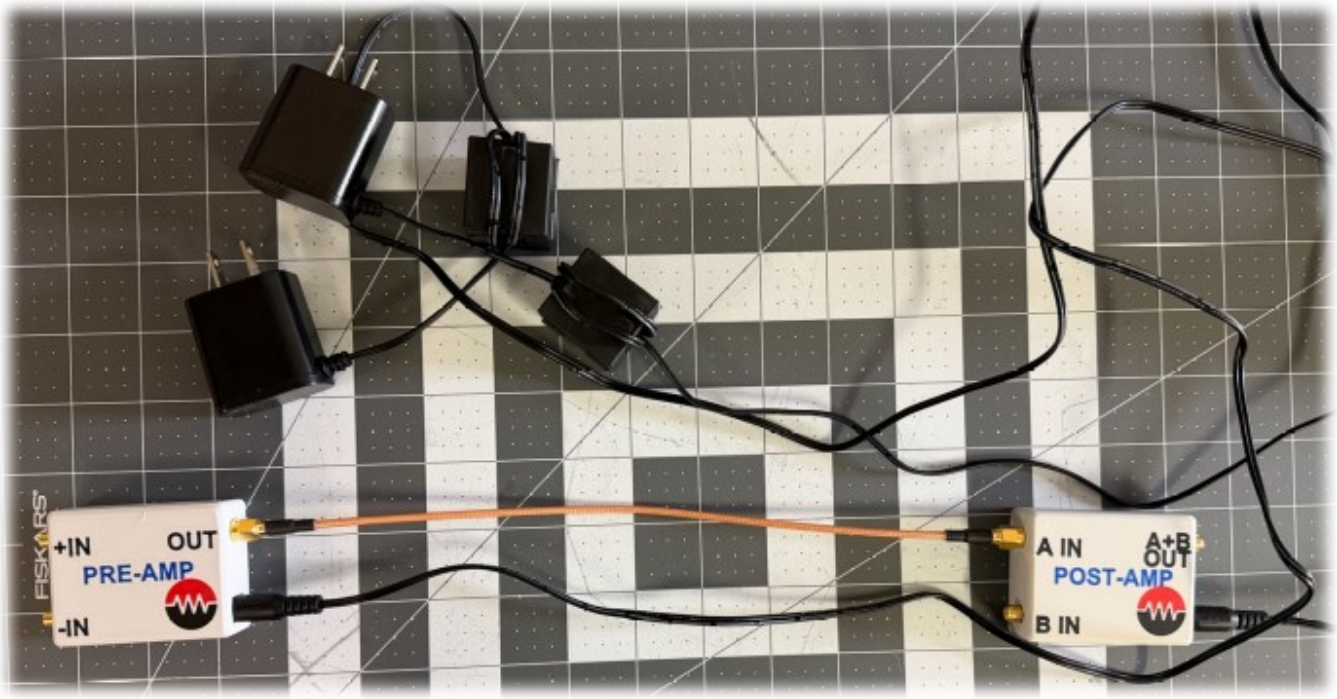
Low-Noise Differential Preamplifier System for FTICR Mass Spectrometry



1. System Overview

The FTICR Pre-Amp System is a two-module, ultra-low-noise signal amplification system designed for Fourier Transform Ion Cyclotron Resonance (FTICR) mass spectrometry detection. The system amplifies the weak differential signal from the FTICR detection cell with minimal added noise, maximizing signal-to-noise ratio for high-resolution mass analysis.

1.1 System Architecture

The system consists of two modules connected in series:

- Pre-Amp Module (Rev 3.0) — High-gain, ultra-low-noise differential amplifier
- Post-Amp Module (Rev 1.0) — Fixed-gain output buffer with optional two-channel summing

Parameter	Value	Notes
Pre-amp differential gain	~210	Pre-amp only, differential input
Pre-amp single-ended gain	~105	Pre-amp only, signal on one input
Post-amp gain	×10	Fixed, non-inverting (separate stage for stability)
System differential gain	~2,100	Pre-amp × post-amp, differential input
System single-ended gain	~1,050	Pre-amp × post-amp, signal on one input
Input referred noise	~1.8 nV/√Hz	Measured, 500 kHz–3 MHz
Theoretical noise floor	1.41 nV/√Hz	√2 × IF1320 device limit
3 dB bandwidth	15 kHz – 3.8 MHz	Full system
CMRR at 100 kHz	>103 dB	Measured
Input impedance	1 GΩ (each gate)	Shunted by gate capacitance at frequency
Output impedance	50 Ω	Matched to coaxial cable
Power supply	24 VDC	CUI SW125-24-N-P5 wall supply
Supply current	~5 mA (pre-amp core)	At optimal 2.5 mA/device bias point

1.2 Intended Application

This system is designed to amplify the ion cyclotron resonance image current signal detected at the FTICR cell electrodes. The differential topology provides excellent rejection of common-mode interference from the magnet power supply, vacuum system electronics, and other laboratory noise sources that couple equally to both detection electrodes.

> **NOTE:** All measurements in this manual were made on a fully assembled system (one pre-amp module + one post-amp module) using a Rigol RSA3015E-TG spectrum analyzer with RBW = 100 Hz and VBW = 100 Hz unless otherwise noted.

2. Pre-Amp Module (Rev 3.0)

2.1 Circuit Description

The pre-amp uses an IF1320/IF4500 JFET cascode differential topology — one of the lowest-noise circuit configurations available for high-impedance signal sources. The design consists of three functional stages:

2.1.1 Input Differential Pair (Q1, Q5 — IF1320)

The two IF1320 N-channel JFETs form the input differential pair. These devices were selected for their exceptionally low voltage noise of 1.0 nV/√Hz typical. Operating at 2.5 mA drain current per device (5 mA total tail current), each device achieves maximum transconductance for minimum noise. The two 1 GΩ gate resistors (R5, R11) provide DC bias return paths while presenting negligible loading to the signal source across the operating frequency band. Gate resistor Johnson noise is filtered by the gate capacitance and is negligible above 15 kHz.

2.1.2 Cascode Stage (Q2, Q4 — IF4500)

The IF4500 P-channel JFETs are connected as cascode devices above Q1 and Q5. The cascode configuration eliminates the Miller effect on the IF1320 gate-drain capacitance, preserving bandwidth and maintaining low effective input capacitance (~1–5 pF as seen by the signal source). The IF4500 devices contribute negligible input-referred noise due to the high impedance at the IF1320 drain nodes.

2.1.3 Tail Current Source (Q3 — IF1320)

A third IF1320 configured as a constant-current source sets the tail current of the differential pair. The 2 kΩ trimmer (R7) allows adjustment of the tail current to optimize the gain and noise performance. The 0.1 µF bypass capacitor (C12) on the current source node provides AC bypassing at very low frequencies (corner ~80 Hz). Current source noise appears as common-mode signal and is largely rejected by the differential pair CMRR.

2.1.4 Output Stage (IC2 — AD8065)

The AD8065 FET-input operational amplifier buffers the differential output of the cascode stage and provides the final voltage gain. Configured with 1 kΩ input resistors (R15, R16) and 10 kΩ feedback resistors (R17, R18), it provides a gain of 10 in a differential-to-single-ended configuration. The 47 Ω output resistor (R19) and series 1 µF capacitor form an AC-coupled 50 Ω output stage for driving the interconnecting coaxial cable.

2.1.5 Power Supply Regulation

The TLE2426CD (IC1) virtual ground generator splits the 24 VDC supply into symmetric ±12 V rails (±UB). The 1N4004 diode (D1) provides reverse-polarity protection. The PTCFUSE (F1) provides overcurrent protection. Bulk decoupling (C1: 10 µF, C5/C8: 1 µF) and local bypass capacitors (C4/C6/C7/C10: 0.1 µF) filter supply noise at all active devices.

2.2 Input Connections

Connector	Signal	Description
J1 (SMA)	+ Input	Non-inverting differential input
J2 (SMA)	− Input	Inverting differential input
J3 (SMA)	Output	Single-ended 50 Ω output to post-amp
PWR	24 VDC	2.1 mm barrel jack, center positive

> **NOTE:** When connecting to the FTICR detection cell, the + input (J1) should be connected to the detection electrode and the − input (J2) to the opposite guard/reference electrode. Reversing the inputs inverts the output signal polarity but does not affect performance.

2.3 Bias Adjustment

The 2 kΩ trimmer R7 adjusts the tail current source to optimize noise performance. The factory-optimized setting is approximately 5 mA total tail current (2.5 mA per device), determined by monitoring the noise floor while increasing current until the noise floor stops decreasing.

Adjustment Procedure

1. Connect a spectrum analyzer to the output (J3) with RBW = 100 Hz, VBW = 100 Hz.
2. Short both inputs (J1 and J2) to ground.
3. Note the noise floor level in dBµV at a frequency between 100 kHz and 1 MHz.
4. Adjust R7 while monitoring the noise level. Noise will drop as current increases, then flatten. Set to the point where noise just stops dropping.
5. Verify gain is within specification using the tracking generator.

3. Post-Amp Module (Rev 1.0)

3.1 Circuit Description

The post-amp provides a fixed gain of ×10 using an AD8065 FET-input operational amplifier. It accepts up to two pre-amp outputs and can sum them for dual-cell or dual-channel FTICR configurations. Gain is set by the ratio of feedback resistor (R8: 10 kΩ) to input resistor (R6: 1 kΩ).

3.2 Input Connections

Connector	Signal	Description
J1 (SMA)	Input A	Primary input — always use for single pre-amp
J2 (SMA)	Input B	Secondary input for second pre-amp (optional)
J3 (SMA)	Output	Summed output, 50 Ω
JP1	Input B Polarity	Selects + or − for Input B
PWR	24 VDC	2.1 mm barrel jack, center positive

NOTE: If only one pre-amp is used, always connect it to Input A (J1). Terminate Input B (J2) with a 50 Ω terminator if not in use. JP1 sets Input B polarity: + is non-inverting, − is inverting.

3.3 Single vs. Dual Pre-Amp Configuration

Configuration	Connection	Use Case
Single pre-amp	Pre-amp out → Input A	Standard single-cell FTICR detection
Dual pre-amp (summing)	Pre-amp 1 → Input A Pre-amp 2 → Input B, JP1 = +	Dual-cell or differential cell
Dual pre-amp (differencing)	Pre-amp 1 → Input A Pre-amp 2 → Input B, JP1 = −	Rejects common-mode between cells

4. Measured Performance

4.1 Gain

Parameter	Value	Condition
Pre-amp single-ended gain	~105	Pre-amp only, signal on one input, other grounded
Pre-amp differential gain	~210	Pre-amp only, differential input
Post-amp gain	×10	Fixed, non-inverting
System single-ended gain	~1,050	Pre-amp × post-amp, signal on one input
System differential gain	~2,100	Pre-amp × post-amp, differential input
Gain flatness	±1 dB	15 kHz – 3 MHz
Lower −3 dB point	~15 kHz	AC coupling limited
Upper −3 dB point	~3.8 MHz	Set by drain load RC pole

NOTE: The pre-amp and post-amp are intentionally separate modules with independent gain stages. Combining all gain into a single stage at these noise and gain levels creates stability challenges. The two-module architecture allows the high-gain JFET cascode stage to be located at the detection cell while the post-amp can be located remotely, connected via 50 Ω coaxial cable.

4.2 Noise Performance

Input-referred noise was characterized using two independent methods that bracket the true performance:

Method	Input Referred Noise	Notes
SA spectral density (shorted inputs)	~1.80–1.90 nV/√Hz	Flat region 500 kHz–3 MHz, system gain 2,100
Scope RMS + bandwidth	~1.34–1.38 nV/√Hz	3.6 mV rms output, 5.95 MHz noise BW
Theoretical limit (2 × IF1320)	1.41 nV/√Hz	√2 × 1.0 nV/√Hz device spec

The amplifier is operating at or very near the theoretical device limit for two IF1320 JFETs in a differential pair. The difference between the two measurement methods reflects inclusion of narrowband interference spurs in the SA integrated measurement.

4.3 Noise Spectral Characterization

Figure 1 shows the measured noise spectra from 10 kHz to 3 MHz for both shorted-input and open-input conditions, along with the derived input-referred voltage noise and current noise across frequency.

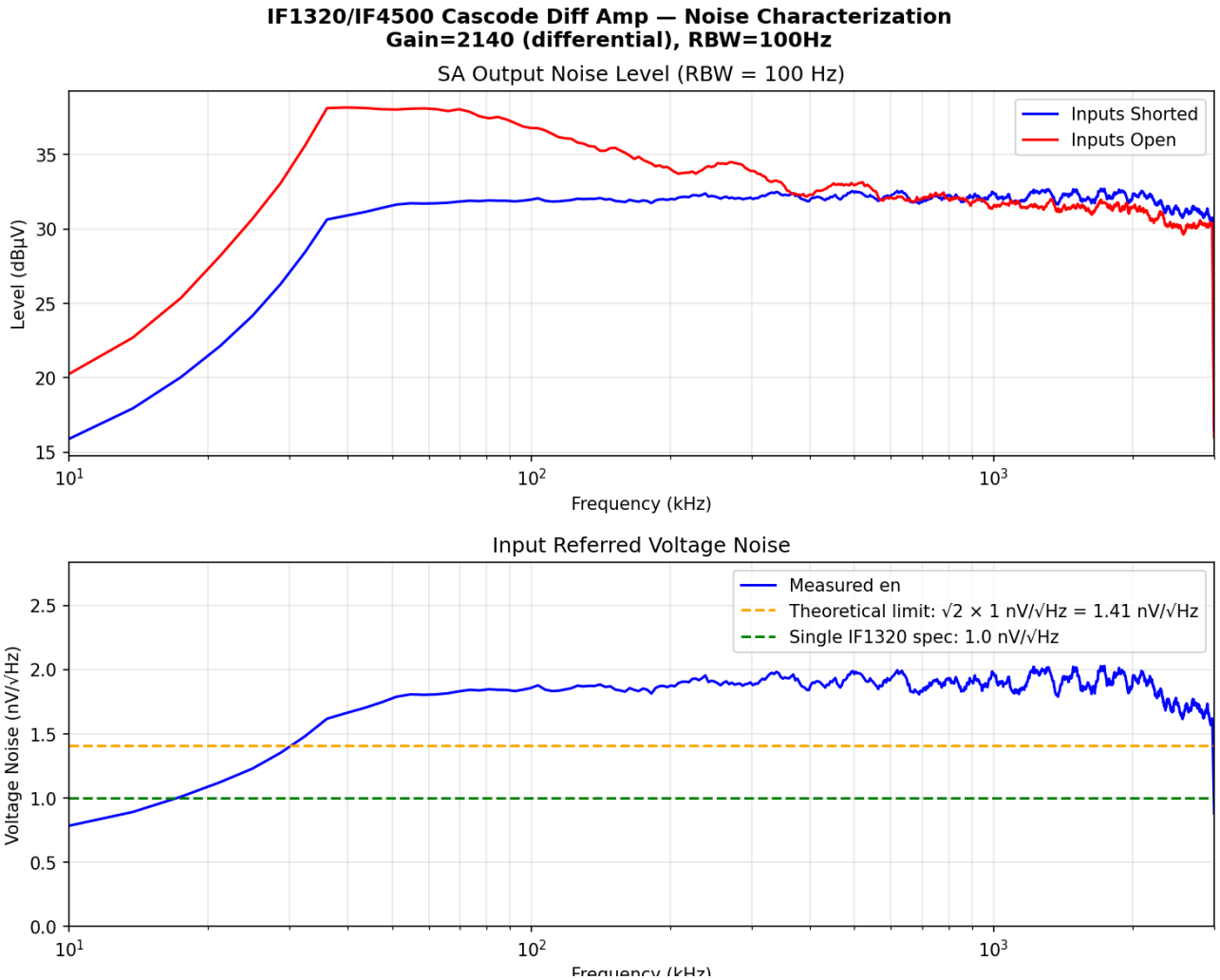


Figure 1a: SA output noise spectra (top) and derived input-referred voltage noise density (bottom). Orange dashed line: theoretical √2 × IF1320 limit (1.41 nV/√Hz). Green dashed line: single device spec (1.0 nV/√Hz). Gain = 2,140 differential. RBW = 100 Hz.

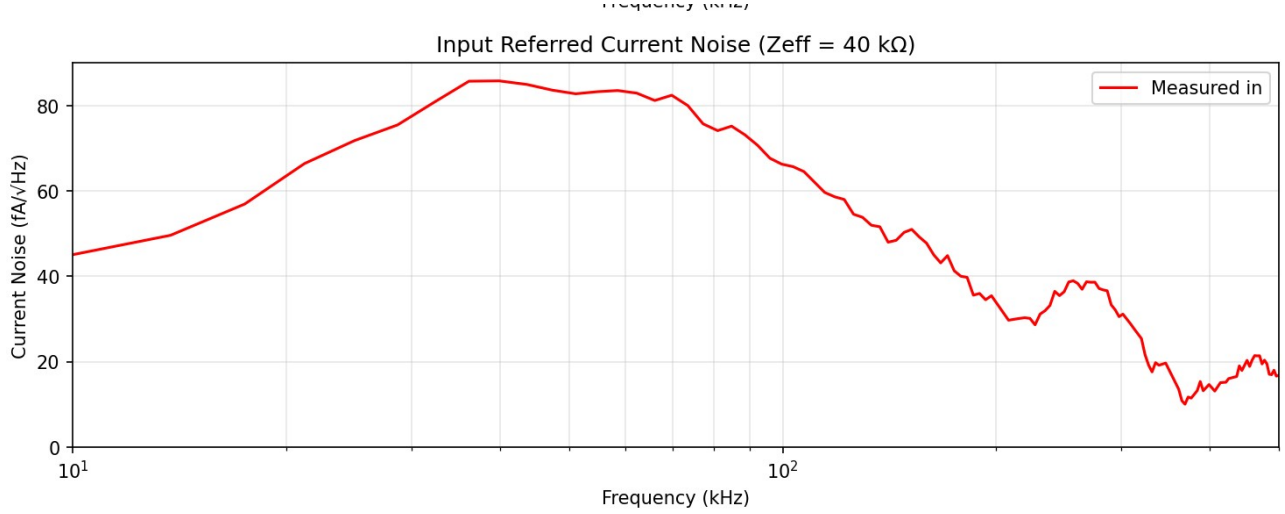
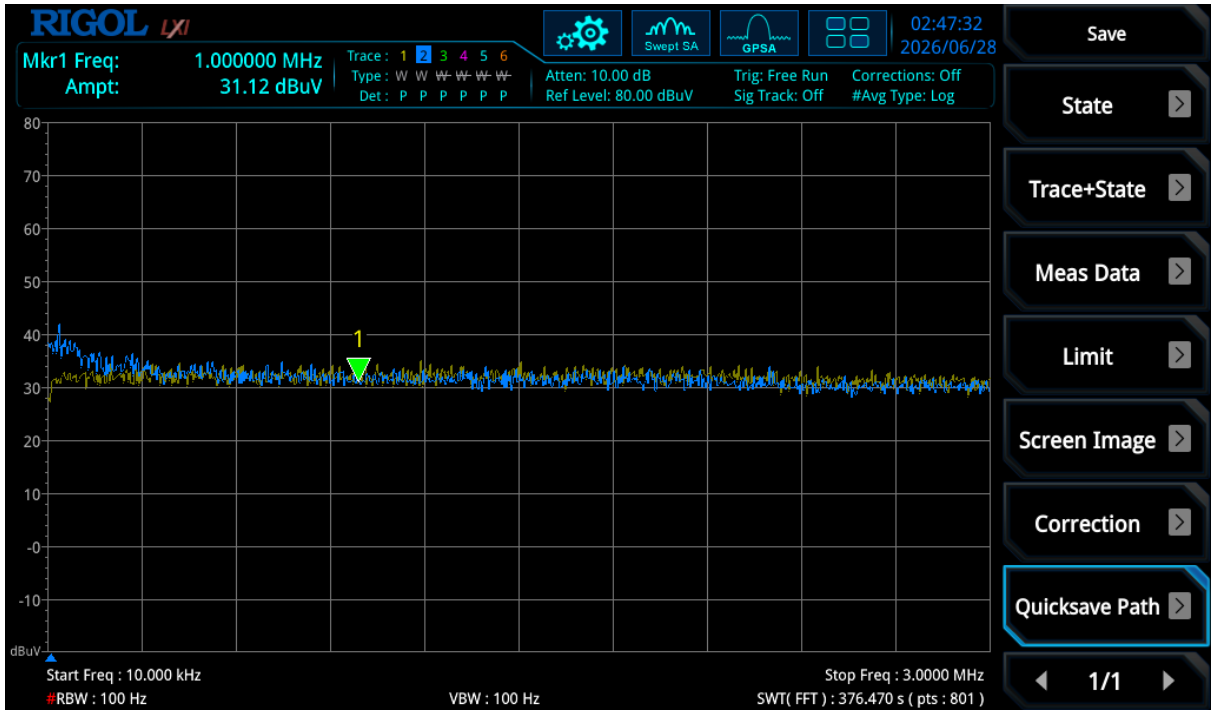


Figure 1b: Input-referred current noise density vs frequency. Current noise is significant below ~358 kHz due to gate leakage 1/f noise × effective source impedance (~40 kΩ). Negligible above 500 kHz.

Key observations from Figure 1:

- Noise floor is flat from 500 kHz to 3 MHz — pure thermal/shot noise, no 1/f contribution within the operating band
- 1/f noise corner is below 10 kHz — outside the FTICR operating band entirely
- Open-input noise is ~8.5 dB higher than shorted at 10 kHz, converging at ~358 kHz — classic gate current noise signature
- Measured voltage noise of ~1.84 nV/√Hz is within 2 dB of the theoretical IF1320 differential pair limit



This plot illustrates the output voltage when the inputs are shorted (yellow trace) and when they are open (blue trace). Notably, the frequency spectrum from 10 kHz to 3 MHz reveals no frequency spurs.

4.4 Current Noise

Parameter	Value	Notes
Open/shorted noise crossover	~358 kHz	From SA spectral data
Excess noise at 10–30 kHz	~8.5 dB	Above shorted-input noise floor
Effective source impedance (Zs)	~40 kΩ	Back-calculated from crossover frequency
Input current noise (10–30 kHz)	~84 fA/√Hz	Derived from Zs and excess noise
1 GΩ gate resistor contribution	Negligible above 15 kHz	Filtered by gate-source capacitance

NOTE: For FTICR cyclotron signals above 358 kHz, the amplifier operates at its pure voltage noise floor with no current noise penalty. For signals below 358 kHz, the effective source impedance of the detection cell will determine the current noise contribution to system SNR.

4.5 Common Mode Rejection Ratio (CMRR)

Parameter	Value	Condition
Common-mode input	204 mV rms	100 kHz sine wave
Common-mode output	3.16 mV rms (70 dBµV)	Measured on SA
Common-mode gain (Acm)	0.0155	3.16 mV / 204 mV
Differential gain (Adiff)	2,100	Measured
CMRR at 100 kHz	>103 dB	20×log(Adiff / Acm)

NOTE: CMRR degrades with increasing frequency due to parasitic capacitance imbalances between the two signal paths. Measure CMRR at the specific frequencies of interest in your FTICR application. The 103 dB result at 100 kHz is expected to degrade to 40–60 dB at 3 MHz.

5. Installation and Setup

5.1 Required Equipment

- CUI SW125-24-N-P5 24 VDC wall supply (one per module)
- SMC coaxial cable, 24" (supplied) for pre-amp to post-amp connection
- 50 Ω coaxial cable for post-amp output to data acquisition system
- 50 Ω SMA terminator for unused Post-Amp Input B

5.2 Single Pre-Amp Setup

6. Mount the pre-amp module as close to the FTICR detection cell as physically possible to minimize lead length and stray pickup.
7. Connect the FTICR cell + electrode to J1 (+ input) and − electrode to J2 (− input) using short shielded cable.
8. Connect pre-amp J3 (output) to post-amp J1 (Input A) using the supplied 24" SMC coaxial cable.
9. Terminate post-amp J2 (Input B) with a 50 Ω SMA terminator.
10. Connect post-amp J3 (output) to your data acquisition system input.
11. Connect 24 VDC supply to both modules. The LED on each module will illuminate when powered correctly.

5.3 Shielding and Grounding

At the gain levels of this system, shielding and grounding are critical for achieving specified noise performance:

- Mount pre-amp in a metal enclosure bonded to instrument chassis ground
- Keep input leads as short as possible — unshielded leads will pick up interference at this gain
- Use single-point grounding to avoid ground loops between pre-amp, post-amp, and DAQ
- If interference is visible on the SA, check the pre-amp enclosure is fully sealed with no apertures facing the magnet power supply

6. Operation and Verification

6.1 Noise Floor Verification

Measurement	Expected Result	Setting
Output noise, inputs shorted	~30 dBµV	SA: RBW = VBW = 100 Hz
Output noise, inputs open (shielded)	~8–9 dB higher at 10 kHz	Same
Open/shorted convergence	~358 kHz	Observe SA spectrum
Scope RMS noise (inputs shorted)	~3.5–4.0 mV rms	20 MHz BW, no limit

6.2 Gain Verification (SA Method)

The most accurate SA-based method uses dBµV subtraction, which cancels SA calibration offset:

12. Apply a signal through >60 dB precision attenuation to one pre-amp input. Ground the other input.
13. Measure input level at the pre-amp input in dBµV.
14. Measure output level at the post-amp output in dBµV.
15. Gain (dB) = Output (dBµV) − Input (dBµV). Expected: ~80 dB single-ended.

> **NOTE:** Never drive the pre-amp input directly from a tracking generator without attenuation. The TG minimum output of −20 dBm produces ~9 V rms at the pre-amp output — sufficient to damage the circuit. Always use at least 60 dB of attenuation.

7. Key Component Reference

7.1 Pre-Amp Module

Ref	Value / Part	Function
Q1, Q5	IF1320 (N-ch JFET)	Input differential pair — primary noise-determining devices
Q2, Q4	IF4500 (P-ch JFET)	Cascode stage — eliminates Miller effect, preserves BW
Q3	IF1320 (N-ch JFET)	Tail current source
Q6, Q7	IF1320 (N-ch JFET)	Additional bias/mirror devices
IC2	AD8065	Output buffer and gain stage (gain = 10)
IC1	TLE2426CD	Virtual ground / rail splitter (±12 V from 24 V)
R5, R11	1 GΩ	Gate bias resistors (noise filtered by gate capacitance)
R6, R9	1.5 kΩ	JFET drain load resistors (sets gain + upper BW)
R7	2 kΩ trimmer	Tail current adjustment
R8	27 Ω	Current source resistor — sets tail current level
R15, R16	1 kΩ	AD8065 input resistors
R17, R18	10 kΩ	AD8065 feedback resistors
R19	47 Ω	Output series resistor (AC-coupled 50 Ω output)
C12	0.1 µF	Current source bypass
D1	1N4004	Reverse polarity protection
F1	PTCFUSE	Overcurrent protection
J1, J2, J3	SMA	Input (+/−) and output connectors

7.2 Post-Amp Module

Ref	Value / Part	Function
IC2	AD8065	Summing amplifier, gain ×10
IC1	TLE2426CD	Virtual ground / rail splitter
R6, R7	1 kΩ	Input A and B summing resistors
R8, R9	10 kΩ	Feedback and gain-setting resistors
R5	1 kΩ	Input B polarity path
R10	47 Ω	Output series resistor
JP1	2-position jumper	Input B polarity select (+ or −)
J1, J2	SMA	Input A and B connectors
J3	SMA	Output connector
D1	1N4004	Reverse polarity protection

F1	PTCFUSE	Overcurrent protection

8. Troubleshooting

Symptom	Likely Cause	Remedy
LED not illuminated	No power or wrong polarity	Check supply polarity and voltage (24 VDC)
No output signal	Connection or power issue	Verify all SMA connections; check LED
Noise floor >35 dBµV (shorted inputs)	Oscillation or interference pickup	Check shielding; verify tail current
Noise elevated open vs. shorted inputs	Normal — current noise × source impedance	Expected ~8 dB higher at 10 kHz; see Section 4.4
CMRR degraded	Input path asymmetry	Check cable lengths to cell are equal
Gain low (~500 instead of ~1,050)	SA input overload / attenuation error	Check SA attenuation setting
Oscillation	Capacitive load or ground instability	Add ferrite bead on output; check ground
60/120 Hz hum	Ground loop	Use single-point ground; check shield continuity

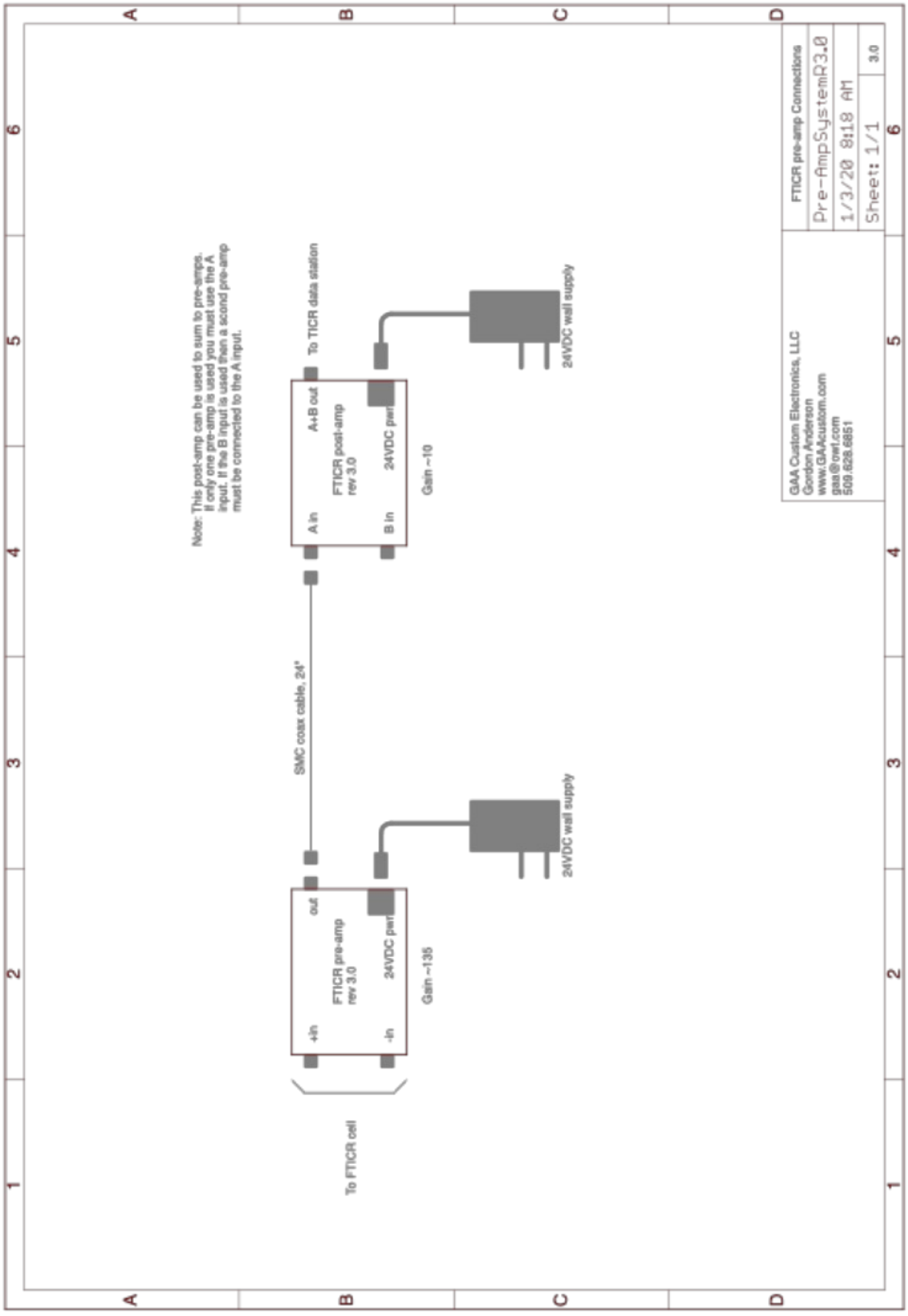
9. Complete Electrical Specifications

Pre-Amp Module (Rev 3.0)

Parameter	Min	Typical	Max	Units
Pre-amp differential gain	—	210	—	V/V
Pre-amp single-ended gain	—	105	—	V/V
System differential gain (with post-amp)	—	2,100	—	V/V
System single-ended gain (with post-amp)	—	1,050	—	V/V
Lower −3 dB frequency	—	15	—	kHz
Upper −3 dB frequency	—	3.8	—	MHz
Input referred voltage noise	—	1.8	—	nV/√Hz
Input referred current noise	—	84	—	fA/√Hz
1/f corner frequency	—	<10	—	kHz
CMRR at 100 kHz	100	103	—	dB
Input impedance (each gate)	—	1	—	GΩ
Output impedance	—	50	—	Ω
Supply voltage	22	24	26	VDC
Supply current (core)	—	5	—	mA
Optimal drain current / device	—	2.5	—	mA
Operating temperature	0	25	50	°C

Post-Amp Module (Rev 1.0)

Parameter	Min	Typical	Max	Units
Voltage gain	—	10	—	V/V
Input impedance (each input)	—	1,000	—	Ω
Output impedance	—	50	—	Ω
Supply voltage	22	24	26	VDC
Number of inputs	—	2	—	—
Input B polarity	—	JP1 selectable	—	+ or −



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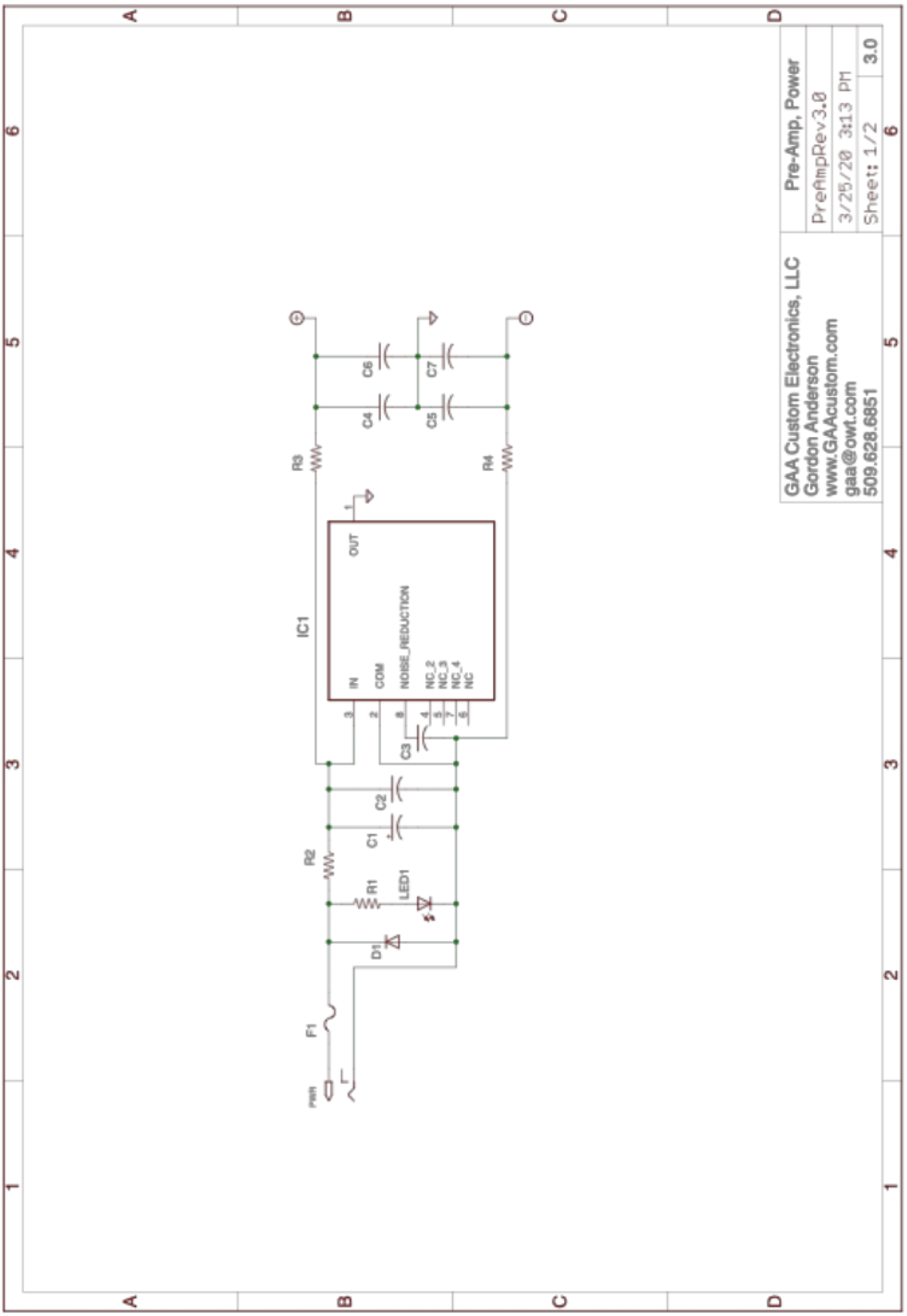
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NC_3
NC_4
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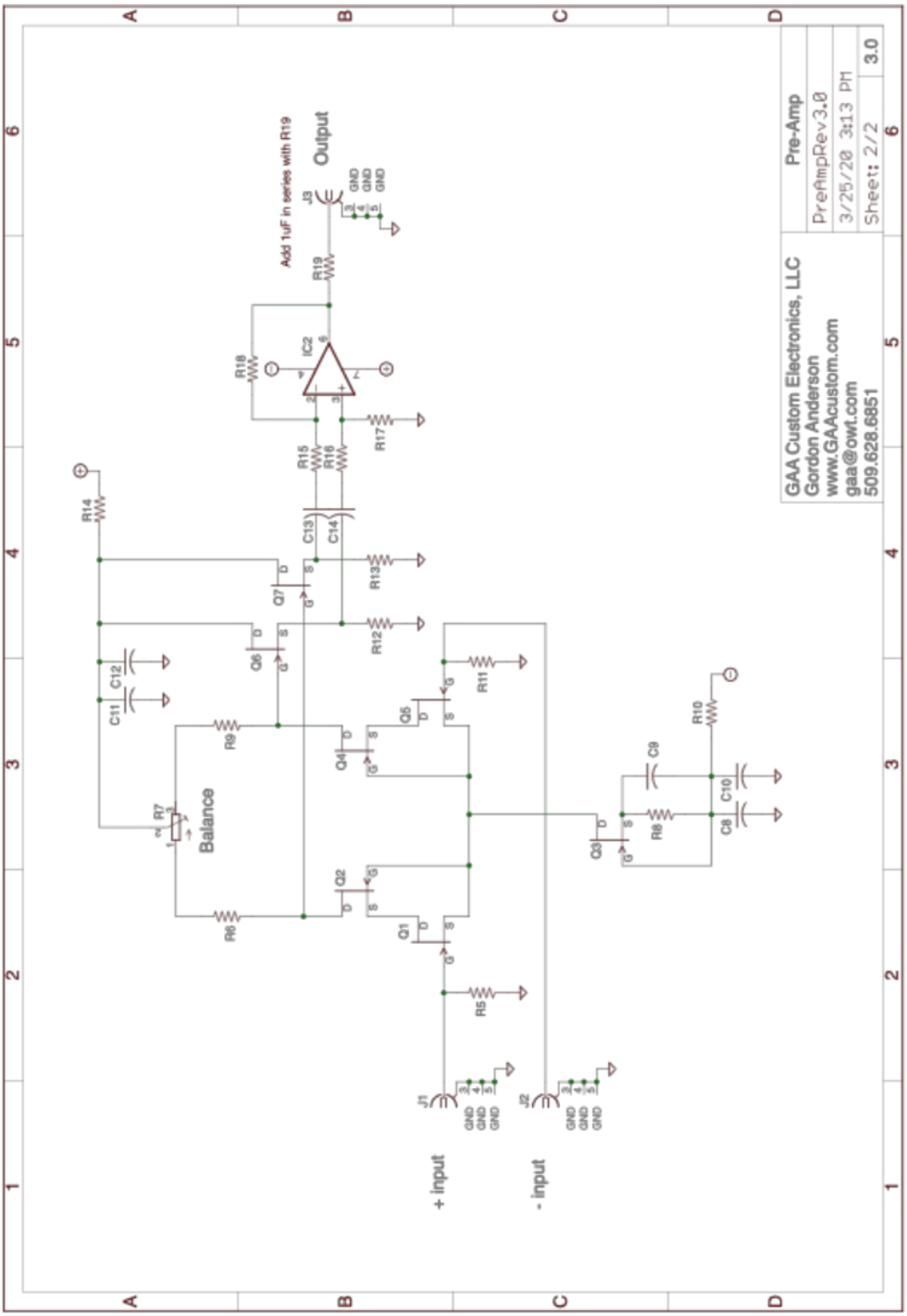
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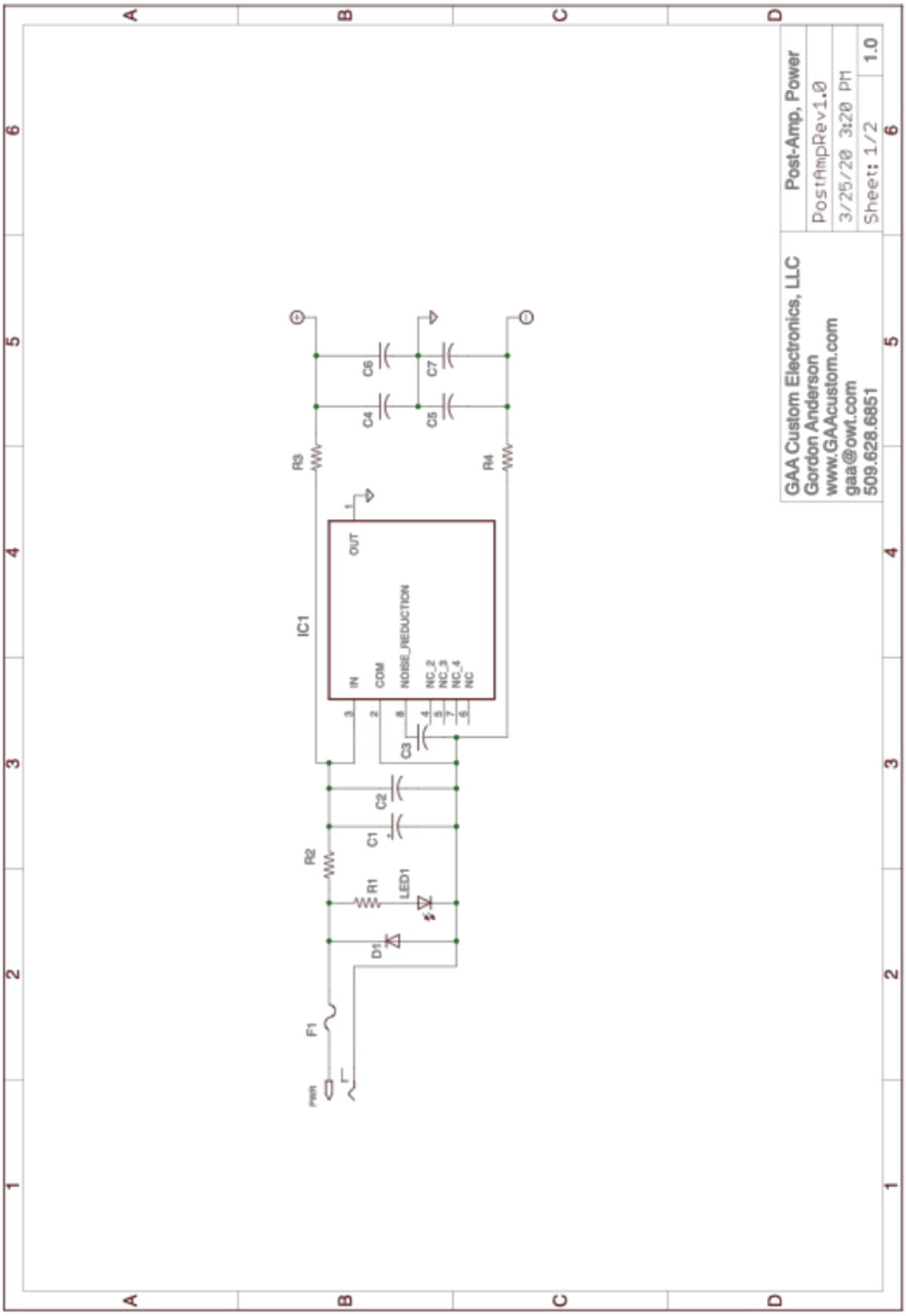
Output
Add 1uF in series with R19
+ input
- input
Balance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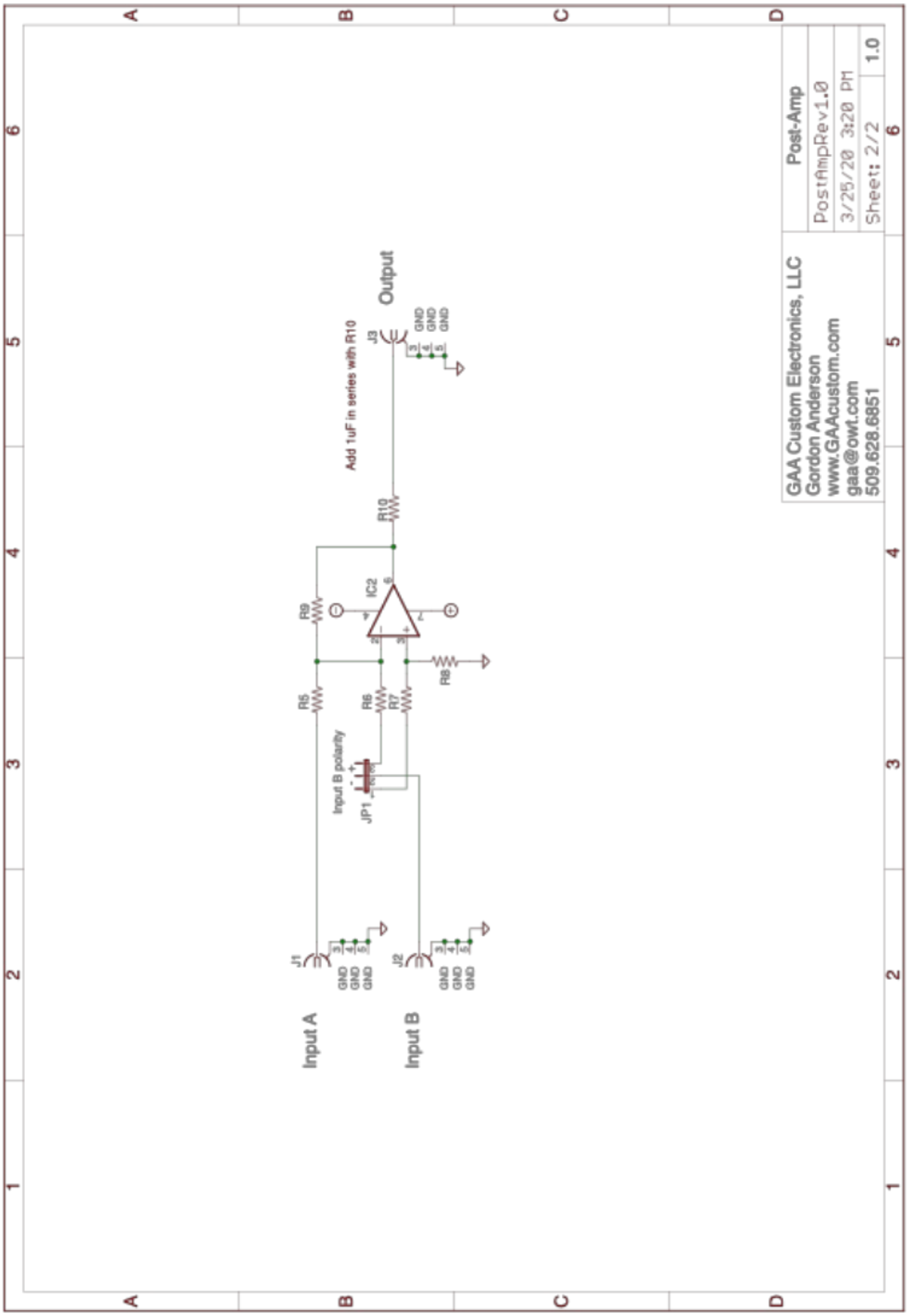
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Output
J3
GND
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GND
Add 1uF in series with R10
R10
IC2
R9
R8
R5
R6
R7
Input B polarity
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Input A
Input B