MIPS

Operations Manual

Rev 4.0 | Firmware v1.262+

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Revision History

Revision	Date	Description
1.0	2015	Initial firmware release — basic DC bias, RF driver, Twave
1.11	Jan 2018	Updated for firmware v1.40; added QUAD and FAIMS appendices
3.0	Mar 2026	Complete rewrite for firmware v1.262; all 648 commands documented; new modules ARB v5, RF QUAD, LDM, FAIMSfb, HOFAIMS, DC Bias pulse mode, high-speed ADC, WiFi/Ethernet
4.0	Mar 2026	Integrated all addenda as chapters; added ARB alternate waveform commands, RF QUAD auto-tune commands, enhanced FAIMS CV scan commands; published as unified manual

1 Safety

> **⚠ WARNING**
> HIGH VOLTAGE HAZARD — Modules including ESI (up to ±8,000 VDC), FAIMS (up to 5,500 Vp-p RF), and RF QUAD operate at voltages lethal on contact. Always de-energize the system before making or removing cable connections.

1.1 Electrical Hazards

The MIPS system contains high-voltage modules that generate voltages exceeding safe human contact limits. All connections must be made with power removed and with appropriate insulating tools. High-voltage cables and connectors supplied with the system are rated for the voltages involved and must not be substituted.

- Never touch output connectors or cabling while any power supply is enabled.
- Verify that all HV outputs read 0 V before connecting or disconnecting any load.
- Use the ESI disable (SHVDIS) and FAIMS enable flag (SFMENA,FALSE) before servicing.
- RF output power from the FAIMS module presents additional burn hazard. Allow 5 minutes after RF shutdown for the RF deck to cool.

1.2 Environmental Requirements

Operating temperature	0 °C to 40 °C
Storage temperature	−20 °C to 60 °C
Humidity	5 % to 85 % non-condensing
Altitude	Up to 2,000 m (6,562 ft) above sea level
Ventilation	Minimum 10 cm clearance on all vented panels; do not block intake fan
Power input	100–240 VAC, 50/60 Hz; fuse rating per rear-panel label

1.3 Module-Specific Safety

1.3.1 FAIMS Module

> **⚠ WARNING**
> The FAIMS module generates asymmetric RF at up to 5,500 Vp-p. The RF deck must be fully enclosed during operation. An emergency OFF button is located on the RF deck front panel.

- Do not connect or disconnect FAIMS HV cables while RF is enabled.
- Inspect all RF connectors and insulation annually.
- Disable arc detection only under direct supervision (SARCDIS,TRUE); re-enable immediately after.

1.3.2 ESI Module

> **⚠ WARNING**
> ESI module output voltages range up to ±8,000 VDC. The positive-supply and negative-supply commands (SHVPSUP, SHVNSUP) accept voltages in this range. Always confirm the ESI is disabled (SHVDIS) before connecting spray emitters.

1.3.3 RF Driver and RF QUAD

RF Driver and RF QUAD modules generate RF power for ion guides and quadrupoles respectively. Output frequencies are typically 400 kHz to 2 MHz.

- Ensure loads are properly matched before enabling RF.
- Do not operate with open-circuit RF output (no load).
- Use auto-tune (SRFATUNE or SRFATUNER) only with the load connected.

1.4 Emergency Procedure

1. Press the front-panel power button to cut all module power.
2. Issue SDCPWR,OFF to disable DC bias outputs via software.
3. Issue SHVDIS to disable ESI output.
4. Issue SFMENA,FALSE to disable FAIMS RF.
5. Wait a minimum of 5 minutes before touching any high-voltage connection.

2 Introduction

The Modular Intelligent Power Supply (MIPS) is a highly configurable laboratory power supply platform designed for mass spectrometry, ion mobility, and related analytical instrumentation. It is controlled by an ARM Cortex-M3 processor (Atmel SAM3X8E on Arduino Due form factor) and communicates with a host computer via USB, Wi-Fi, or Ethernet using a simple ASCII command protocol.

Modules are discovered automatically at power-on by scanning the I²C (TWI) bus for recognised EEPROM signatures. Each module registers its menu entries, initialisation routines, and serial commands with the MIPS kernel; no manual configuration of the controller is required when adding or removing modules.

2.1 System Architecture

Component	Description
Controller	Arduino Due (ARM SAM3X8E, 84 MHz Cortex-M3, 96 KB SRAM, 512 KB Flash)
Display	2.2" TFT colour LCD (ILI9340 or H8347), 320×240 pixels
User input	Single rotary encoder with push-button
Storage	Micro-SD card (FAT32), stores configuration, macros, firmware images
Host interface	Native USB (CDC-ACM), optional Wi-Fi (ESP8266), optional Ethernet (USR-TCP232-T2)
Module bus	I²C (TWI) at up to 400 kHz for all modules; SPI for DAC updates
Max modules	8 module slots (4 per board-select × 2 board-selects A/B), each addressed 0x50–0x56
Expansion	Up to 32 DC bias channels, 6 ARB modules (48 outputs), 4 RF driver channels, 2 Twave modules, 2 ESI channels, 1 FAIMS/HOFAIMS/FAIMSfb, 1 RF QUAD, 1 LDM

2.2 Firmware v1.262 Feature Summary

Key capabilities added since the original v1.40 manual:

- 357+ serial commands covering all installed modules
- Wi-Fi (ESP8266) and Ethernet (USR-TCP232-T2) host interfaces
- DC bias profiles (up to 10) with toggle and dwell timing
- DC bias pulse mode — per-channel voltage pulses with programmable timing
- High-speed ADC vector recording (up to 100 kHz, up to 4 channels)
- ARB v5: 6-module support, alternate waveform, PPP control, dual-board offsets, ARB-level sweep
- RF QUAD: m/z-based scan, auto-tune with SWR optimization, frequency compensation
- FAIMS: CV scan, arc detect calibration, HOFAIMS and FAIMSfb variants
- Level Detection Module (LDM) for analogue-triggered ARB delay/duration control
- SD card file management (DIR, DEL, GET, PUT), EEPROM save/restore (SAVEMOD, LOADMOD, SAVEALL, LOADALL)
- Macro record/playback system
- UUID reporting, CPU temperature, trace/debug system

3 User Interface

The MIPS front panel consists of a colour TFT display and a single rotary encoder with integral push-button. All operational parameters are accessible through the front-panel menu hierarchy; host-computer commands mirror every UI function.

3.1 Display and Encoder

- Rotate the encoder to highlight a menu item or change a value.
- Press the encoder to select/confirm a highlighted item.
- Rotating quickly while adjusting a numeric value applies coarse steps.
- The LED button on some configurations illuminates: blue = outputs active above 0 V; red = any output > 50 V; flashing red = any output > 100 V.

3.2 Main Menu

On power-on the main menu lists installed modules in discovery order plus the built-in MIPS Configuration and About entries. Scroll with the encoder and press to enter a module's control menu.

3.3 MIPS Configuration

Parameter	Description/Range
Controller rev	Hardware revision 1–10; set to match PCB revision
Startup delay	1–100 ms delay before module init; default 10 ms
Startup hold	YES = hold for button press before loading defaults
DCbias supply	ON/OFF — enables or disables the DC bias board power supply
DCbias trip, %FS	0–100 % — voltage error threshold triggering supply trip; default 5 %
Reboot	Executes a firmware software reset
Backlight, %	5–100 % — adjusts TFT backlight brightness
Macro options	Select a macro to play at startup; record/playback menu
Config modules	Format (re-initialise) module EEPROM; select board address and type

3.4 Save and Restore

The SAVE command writes the current configuration to default.cfg on the SD card. This file is automatically loaded on the next power-on. Use RESTORE to reload from the card without a reboot.

4 Host Computer Interface

The MIPS system accepts ASCII commands from any terminal programme or application that can connect to a USB COM port, TCP/IP socket (Wi-Fi or Ethernet), or Bluetooth serial link.

4.1 Connection

Interface	Settings / Notes
USB (native)	CDC-ACM virtual COM port; no baud rate configuration needed; plug-and-play on Windows 10+, macOS, Linux
USB (hardware UART)	9600 baud, 8-N-1; enabled at compile time via variants.h; used for Bluetooth adapters
Wi-Fi	TCP socket on configured IP:port; see Section 5.1
Ethernet	TCP socket on configured IP:port; see Section 5.2

4.2 Command Protocol

Each command is a single ASCII string terminated by carriage return (\r) or linefeed (\n).

- Command names are case-insensitive.
- Parameters are separated by commas with no spaces.
- Floating-point values accept up to 6 significant digits.
- Acknowledged commands respond: ACK\n\r
- Commands returning a value respond: value\n\r then ACK\n\r (or just value\n\r when MUTE is active)
- Commands with errors respond: NAK\n\r

Example command sequence:

```
SDCB,1,50.0   → sets DC bias channel 1 to 50.0 V; returns ACK
GDCB,1        → returns '50.0' then ACK
GERR          → returns error code (0 = no error)
```

4.3 General Commands

Command	Parameters	Description
GVER	—	Returns firmware version string
GERR	—	Returns last error code (0 = no error; see Appendix B)
GNAME	—	Returns MIPS system name
SNAME	<name>	Sets MIPS system name (up to 20 characters)
UUID	—	Reports 128-bit unique controller ID in hex
ABOUT	—	Reports version, name, Wi-Fi/Ethernet status, and installed modules with addresses and revisions

SMREV	<brd>,<addr>,<rev>	Sets a module's revision level; brd = A or B; addr = hex TWI address
RESET	—	Software reset (reboots firmware)
STATUS	—	Reports last reboot reason and elapsed ms since boot
SAVE	—	Saves current configuration to default.cfg on SD card
GCHAN	<system>	Reports number of channels for the named system (RFDRIVER, DCBias, DIO, etc.)
MUTE	<TRUE|FALSE>	Suppresses ACK/NAK responses when TRUE
ECHO	<TRUE|FALSE>	Enables command echo back to host
TRIGOUT	<mode>	Generates trigger output pulse; mode: WIDTH, FOLLOW, FOLLOWS
DELAY	<ms>	Inserts a delay in milliseconds (used in macros)
GCMDS	—	Returns a comma-separated list of all registered commands
GAENA	—	Returns UseAnalog flag
SAENA	<TRUE|FALSE>	Sets UseAnalog flag
THREADS	—	Lists all running threads with last execution times
STHRDENA	<name>,<TRUE|FALSE>	Enables or disables the named thread
SDEVADD	<brd>,<addr>	Defines the board address for TWI operations
SSPND	<TRUE|FALSE>	Suspends all tasks for real-time control
GSPND	—	Returns suspend status
CPUTEMP	—	Returns CPU junction temperature in °C (not calibrated)
TWITALK	<brd>,<addr>	Redirects serial port to the specified TWI device for direct communication
LEDOVRD	<TRUE|FALSE>	Overrides automatic LED control
LED	<mask>	Sets LED state: bit 0=RED, bit 1=BLUE, bit 2=GREEN, bit 3=blink
DSPOFF	<TRUE|FALSE>	Disables/enables the front-panel display
CHKIMAGE	<file>	Reports status of image file on SD card
LOADIMAGE	<file>	Loads image file to display
SSERIALNAV	<TRUE|FALSE>	Enables host-controlled UI navigation when TRUE
TRACE	—	Enables firmware trace buffer (requires linker modification)
TBLTSKENA	<TRUE|FALSE>	Enables background task execution during table operation
SOFTLDAC	<TRUE|FALSE>	Forces software LDAC for DC bias updates
RDEV	<ch>	Reads ADC channel value from AD7998 device
RDEV2	<ch>	Reads ADC channel value from AD7994 device

4.4 SD Card File Management

Command	Parameters	Description

DIR	—	Lists all files on the SD card with sizes
DEL	<file>	Deletes named file from SD card
GET	<file>	Dumps file contents as hex to host
PUT	<file>,<size>	Receives hex data from host and writes to named file
SAVEMOD	<file>,<brd>,<addr>	Saves module EEPROM (at brd, addr) to named SD file
LOADMOD	<file>,<brd>,<addr>	Loads named SD file to module EEPROM
SAVEALL	—	Saves all discovered module EEPROMs to individual SD files
LOADALL	—	Loads all module EEPROMs from files saved by SAVEALL
GETEEPROM	<brd>,<addr>	Sends EEPROM data to host; brd = A or B; addr = hex TWI address
PUTEEPROM	<brd>,<addr>	Receives data from host and writes to EEPROM

4.5 Macro System

Macros are ASCII text files stored on the SD card. Any sequence of valid MIPS commands can be recorded as a macro and replayed. A macro can be configured to run automatically at system startup.

Command	Parameters	Description
MRECORD	<file>	Begins recording commands to named file; subsequent commands are saved (not executed during recording)
MSTOP	—	Stops recording and closes the macro file
MPLAY	<file>	Plays back the named macro file
MLIST	—	Returns a comma-separated list of all macro files on the SD card
MDELETE	<file>	Deletes the named macro file

4.6 System Diagnostics

Command	Parameters	Description
ADC	<ch>	Reads and reports ARM ADC channel 0–3 (raw 12-bit value)
ADCINIT	—	Configures ADC for vector recording; call before ADCTRIG
ADCTRIG	—	Software trigger for ADC vector acquisition
ADCABORT	—	Aborts a running ADC acquisition
SADCCHAN	<ch>	Sets ADC channel for acquisition
GADCCHAN	—	Returns configured ADC channel
SADCSAMPS	<n>	Sets number of samples per vector
GADCSAMPS	—	Returns sample count
SADCVECTS	<n>	Sets number of vectors to acquire

GADCVECTS	—	Returns vector count
SADCRATE	<Hz>	Sets ADC sample rate in Hz (max ~200 kHz)
GADCRATE	—	Returns sample rate
BIMAGE	<file>	Sets boot image filename to display at startup
ENTEST	—	Tests Ethernet adapter connection

5 Wi-Fi and Ethernet

MIPS supports two IP network options: an ESP8266 Wi-Fi module and a USR-TCP232-T2 Ethernet-to-UART bridge. Both interfaces present a TCP socket on a configurable port and operate identically to the USB interface from the host's perspective.

5.1 Wi-Fi (ESP8266)

The ESP8266 module connects to an existing 2.4 GHz Wi-Fi network (WPA2-PSK). It requires a configured SSID, password, and host name. The module is enabled by the SWIFIENA command and its serial port is selected with SWIFISP.

Command	Parameters	Description
`GHOST`	—	Returns this MIPS box's host name
`SHOST`	<name>	Sets host name
`GSSID`	—	Returns configured Wi-Fi SSID
`SSSID`	<ssid>	Sets Wi-Fi SSID
`GPSWD`	—	Returns Wi-Fi password
`SPSWD`	<password>	Sets Wi-Fi password
`SWIFIENA`	<TRUE|FALSE>	Enables/disables Wi-Fi at next reboot
`SWIFISP`	<0|1>	Sets the UART port (0 or 1) connected to the Wi-Fi module

5.2 Ethernet

The Ethernet adapter communicates over a UART with the MIPS controller and is configured with a static IP address. The adapter is auto-detected at power-on on UART2.

Command	Parameters	Description
`GEIP`	—	Returns adapter IP address
`SEIP`	<ip>	Sets adapter IP address (e.g., SEIP,192.168.1.100)
`GESNIP`	—	Returns subnet mask
`SESNIP`	<ip>	Sets subnet mask
`GEPORT`	—	Returns TCP port number
`SEPORT`	<port>	Sets TCP port number
`GEGATE`	—	Returns gateway IP address
`SEGATE`	<ip>	Sets gateway IP address
`ENTEST`	—	Sends test packet; returns OK if adapter responds

6 RF Driver Module

The RF Driver module generates RF voltages for quadrupole ion guides and ion funnels. Up to four RF channels are supported (two boards × two channels each). Each channel produces an RF output whose amplitude and frequency are independently programmable.

6.1 Specifications

Channels	Up to 4 (2 per board, 2 boards)
Frequency range	50 kHz to 5 MHz (hardware dependent)
Output voltage	Up to 1,500 Vp-p (hardware dependent)
Drive control	0–100 % PWM drive; readback via level sensor
Modes	Manual, Auto (closed-loop), Auto-Tune
Gate input	TTL digital input selectable; active level configurable

6.2 Operating Modes

6.2.1 Manual Mode

In manual mode the user sets the drive percentage directly. Output voltage readback is displayed but does not feed back to the drive control.

6.2.2 Auto Mode (Closed-Loop)

Auto mode uses the RF level sensor to maintain a user-set output voltage. The control loop adjusts the drive percentage at each update cycle.

6.2.3 Auto-Tune

Auto-tune scans frequency to find the resonant peak, then optimises drive for the target output level. Issue SRFATUNE,<ch> or SRFATUNER,<ch> (with console reporting). A TUNE COMPLETE message is returned when complete.

6.3 Host Commands

Command	Parameters	Description
`SRFFRQ`	<ch>,<Hz>	Sets RF frequency in Hz for the selected channel
`GRFFRQ`	<ch>	Returns RF frequency
`SRFDRV`	<ch>,<%>	Sets RF drive in percent (0–100)
`GRFDRV`	<ch>	Returns RF drive
`SRFVLT`	<ch>,<V>	Sets RF output voltage setpoint in volts (auto mode)
`GRFVLT`	<ch>	Returns RF voltage setpoint

GRFPPVP	<ch>	Returns RF positive peak voltage readback
GRFPPVN	<ch>	Returns RF negative peak voltage readback
GRFPWR	<ch>	Returns RF power in watts
SRFMODE	<ch>,<mode>	Sets mode: MANUAL, AUTO
GRFMODE	<ch>	Returns mode
SRFATUNE	<ch>	Starts auto-tune for selected channel
SRFRETUNE	<ch>	Starts retune (1 kHz steps, finer adjustment) for selected channel
SRFCAL	<ch>,<V>,<V>	Sets calibration parameters (positive, negative peak)
SRFHPCAL	<ch>,<V>	Sets positive harmonic peak readback calibration (FAIMS)
SRFHNCAL	<ch>,<V>	Sets negative harmonic peak readback calibration (FAIMS)
SEGATE	<ch>,<in>	Sets RF gate input (Q–X or NA)
GEGATE	<ch>	Returns gate input configuration
SGATERFL	<ch>,<level>	Sets gate active level (POS, NEG, HIGH, LOW)

7 DC Bias Module

The DC bias module provides independent programmable DC voltages for ion optics electrodes. Up to 4 modules (32 channels total) can be installed. Each module provides 8 channels at up to ±250 V standard (±750 V option).

7.1 Host Commands

Command	Parameters	Description
SDCB	<ch>,<V>	Sets voltage setpoint for channel ch
GDCB	<ch>	Returns voltage setpoint
GDCBV	<ch>	Returns actual readback voltage
SDCBOF	<brd>,<V>	Sets float voltage for selected board (A=1, B=2)
GDCBOF	<brd>	Returns float voltage
GDCMIN	<ch>	Returns channel minimum voltage
GDCMAX	<ch>	Returns channel maximum voltage
SDCPWR	<ON|OFF>	Enables/disables DC bias board power supply
GDCPWR	—	Returns power supply state
SDCBALL	<V1,V2,...>	Sets all DC bias channels from comma-separated voltage list
GDCBALL	—	Returns all channel setpoints as comma-separated values
GDCBALLV	—	Returns all channel readback voltages
SDCBDELTA	<ΔV>	Adjusts all channels by the delta value
SDCBCHNS	<brd>,<n>	Sets number of channels on board brd
SDCBONEOFF	<TRUE|FALSE>	Enables use of a single offset DAC for both boards
DCBOFFRBENA	<TRUE|FALSE>	Enables offset readback monitoring
SDCBOFFENA	<ch>,<TRUE|FALSE>	Sets per-channel offset-enable flag
SDCBTEST	<TRUE|FALSE>	Enables/disables readback voltage testing
SDCBADCADD	<brd>,<addr>	Sets ADC TWI address for a board
SDCBARST	<TRUE|FALSE>	Enables automatic trip reset
SDCBRNG	<brd>,<range>	Sets voltage range for a board
SDCBEXT	<brd>	Sets extended addressing mode (factory)

7.1.1 Voltage Profiles

Up to 10 voltage profiles can be stored per MIPS system. A profile is a named set of DC bias setpoints that can be applied instantly, or the system can toggle between two profiles with a programmable dwell time.

Command	Parameters	Description
SDCBPRO	<n>,<V1,V2,...>	Saves a profile: n = profile number 1–10; followed by comma-separated voltages for all channels
GDCBPRO	<n>	Returns the stored profile n as comma-separated voltages

ADCBPRO	<n>	Applies (activates) profile n immediately
CDCBPRO	<n>	Copies current DC bias values into profile n
TDCBPRO	<n1>,<n2>,<dwell_ms>	Toggles between profiles n1 and n2 with dwell_ms milliseconds per profile
TDCBSTP	—	Stops a running profile toggle

7.1.2 Pulse Mode

DC bias pulse mode allows any channel to generate a single voltage pulse: the channel steps to a pulse voltage, holds for a programmable duration, then returns to the pre-pulse setpoint. Useful for ion injection, gating, or timing experiments.

Command	Parameters	Description
SDCBPV	<ch>,<V>	Sets pulse voltage for channel ch
GDCBPV	<ch>	Returns pulse voltage
SDCBPW	<ch>,<µs>	Sets pulse width in microseconds
GDCBPW	<ch>	Returns pulse width
SDCBPT	<ch>,<µs>	Sets pulse period (time between pulses) in microseconds; 0 = single pulse
GDCBPT	<ch>	Returns pulse period
SDCBPD	<ch>,<µs>	Sets pulse delay (from trigger to pulse start) in microseconds
GDCBPD	<ch>	Returns pulse delay
SDCBPENA	<ch>,<TRUE|FALSE>	Enables pulse mode for channel ch
GDCBPENA	<ch>	Returns pulse mode enable state
SDCBPCH	<ch>,<n>	Sets the pulse count (number of pulses); 0 = continuous
GDCBPCH	<ch>	Returns pulse count
SDCBPRO	<brd>	Selects profile for pulse mode output switching
GDCBPRO	<brd>	Returns current pulse profile selection
SDCBSIO	<ch>,<TRUE|FALSE>	Sets per-channel single output mode
GDCBSIO	<ch>	Returns single output mode
SDCBSPWR	<ch>,<TRUE|FALSE>	Sets per-channel power state
GDCBSPWR	<ch>	Returns power state
SDCBSSW	<ch>,<TRUE|FALSE>	Sets switch state for DC bias channel
GDCBSSW	<ch>	Returns switch state
SDCBSTRGSW	<ch>,<TRUE|FALSE>	Sets trigger-controlled switch mode
GDCBSTRGSW	<ch>	Returns trigger switch mode
SDCBSRBTST	<ch>,<TRUE|FALSE>	Sets readback test state per channel
GDCBSRBTST	<ch>	Returns readback test state
SDCBSV	<ch>,<V>	Sets setpoint voltage via alias
GDCBSV	<ch>	Returns setpoint voltage
SDCBS	<ch>,<V>	Sets voltage (alias)
GDCBS	<ch>	Returns voltage (alias)

8 ESI High-Voltage Module

> ⚠ **WARNING**
> ESI module output voltages range up to ±8,000 VDC. Always de-energize before connecting spray emitters.

The ESI module provides high-voltage bias for electrospray ionisation emitters. It supports positive and negative HV independently, current monitoring, over-current trip, voltage ramping, and automatic polarity switching (Rev 3).

8.1 Host Commands

Command	Parameters	Description
SHV	<ch>,<V>	Sets HV output voltage (positive for positive supply, negative for negative)
GHV	<ch>	Returns voltage setpoint
GHVV	<ch>	Returns actual HV readback voltage
GHVI	<ch>	Returns current readback in µA
SHVENA	<ch>	Enables HV output for channel ch
SHVDIS	<ch>	Disables HV output
GHVSTATUS	<ch>	Returns ESI status: ENABLED, DISABLED, TRIPPED
SHVPSUP	<mod>,<V>	Sets positive supply voltage for module mod
SHVNSUP	<mod>,<V>	Sets negative supply voltage for module mod
GHVMAX	<ch>	Returns maximum allowed HV
GHVMIN	<ch>	Returns minimum allowed HV
GHVITST	—	Returns TRUE if current testing is enabled
SHVITST	<TRUE|FALSE>	Enables/disables ESI current over-test
SEIP	<ip>	Sets Ethernet IP (also listed under Ethernet)
SESNIP	<ip>	Sets Ethernet subnet mask

9 Twave Module

The Twave module generates traveling-wave ion mobility separation waveforms. Two modules can be installed and operated together in compressor mode. Hardware revisions 1–5 are supported, with Rev 4+ using a CPLD for clock generation.

9.1 Host Commands

Command	Parameters	Description
STWF	<mod>,<Hz>	Sets Twave frequency in Hz
GTWF	<mod>	Returns frequency
STWPV	<mod>,<V>	Sets pulse voltage in volts
GTWPV	<mod>	Returns pulse voltage
STWG1V	<mod>,<V>	Sets guard 1 voltage
GTWG1V	<mod>	Returns guard 1 voltage
STWG2V	<mod>,<V>	Sets guard 2 voltage
GTWG2V	<mod>	Returns guard 2 voltage
STWSEQ	<mod>,<sequence>	Sets Twave output sequence string
GTWSEQ	<mod>	Returns sequence
STWDIR	<mod>,<FWD|REV>	Sets waveform direction
GTWDIR	<mod>	Returns direction
STBLRBT	<TRUE|FALSE>	Enables Twave readback test

9.1.1 Twave Frequency and Voltage Sweep

The Twave module supports linear sweeps of frequency and pulse voltage. The sweep is initiated by a command or external trigger.

Command	Parameters	Description
STWSSTRT	<mod>,<Hz>	Sets sweep start frequency
GTWSSTRT	<mod>	Returns sweep start frequency
STWSSTP	<mod>,<Hz>	Sets sweep stop frequency
GTWSSTP	<mod>	Returns sweep stop frequency
STWSSTRTV	<mod>,<V>	Sets sweep start voltage
GTWSSTRTV	<mod>	Returns sweep start voltage
STWSSTPV	<mod>,<V>	Sets sweep stop voltage
GTWSSTPV	<mod>	Returns sweep stop voltage
STWSTM	<mod>,<sec>	Sets sweep duration in seconds
GTWSTM	<mod>	Returns sweep duration
STWSGO	<mod>	Starts the sweep
STWSHLT	<mod>	Stops a running sweep
GTWSTA	<mod>	Returns sweep status: IDLE, STARTING, SWEEPING, STOPPING

9.1.2 Twave Compressor (Two-Module Operation)

When two Twave modules are installed, module 2 can be driven in compression mode. The compressor gates module 2's clock for a defined number of cycles to implement CRIMP (Compression Ratio Ion Mobility Programming).

Command	Parameters	Description
STWCMODE	<Normal|Compress>	Sets compressor mode
GTWCMODE	—	Returns compressor mode
STWCORDER	<n>	Sets compression order (1 = normal, >1 = compressed)
GTWCORDER	—	Returns compression order
STWCTBL	<table string>	Sets multi-pass compressor table (see Appendix C)
GTWCTBL	—	Returns compressor table
STWCTD	<ms>	Sets trigger delay in ms
GTWCTD	—	Returns trigger delay
STWCTC	<ms>	Sets compressed-cycle time in ms
GTWCTC	—	Returns compressed-cycle time
STWCTN	<ms>	Sets normal-cycle time in ms
GTWCTN	—	Returns normal-cycle time
STWCTNC	<ms>	Sets non-compressed cycle time in ms
GTWCTNC	—	Returns non-compressed cycle time
TWCTRG	—	Forces a manual compressor trigger
STWCSW	<Open|Close>	Sets compressor ion switch state
GTWCSW	—	Returns switch state
STWCCLK	<TRUE|FALSE>	Enables common clock for two-module synchronisation
STWCMP	<TRUE|FALSE>	Enables Twave compressor mode

10 Filament Module

The Filament module controls thermionic emission current sources. Two channels are supported. Rev 2 hardware allows the channels to be combined for single-channel operation with current-reversal capability. Features include current ramping, duty-cycle cycling, bias-current monitoring, and serial watchdog.

10.1 Host Commands

Command	Parameters	Description
SFLI	<ch>,<A>	Sets filament current setpoint in amperes
GFLI	<ch>	Returns filament current setpoint
GFLAI	<ch>	Returns actual measured filament current
SFLSV	<ch>,<V>	Sets filament supply voltage
GFLSV	<ch>	Returns supply voltage setpoint
GFLASV	<ch>	Returns actual supply voltage
GFLV	<ch>	Returns filament voltage (actual)
GFLPWR	<ch>	Returns filament power in watts
SFLENA	<ch>,<ON|OFF>	Enables/disables filament heating
GFLENA	<ch>	Returns filament enable state
SFLRT	<ch>,<A/s>	Sets current ramp rate in A/s
GFLRT	<ch>	Returns ramp rate
SFLDIR	<ch>,<FWD|REV>	Sets current direction (Rev 2)
GFLDIR	<ch>	Returns current direction
GFLSRES	—	Returns bias current sense resistor value in Ω
SFLSRES	<Ω>	Sets sense resistor value
GFLECUR	—	Returns filament emission current
SFLSWD	<TRUE|FALSE>	Enables/disables serial watchdog: disables filament if no serial traffic
RFLPARMS	<ch>,<rate>	Sets filament parameter reporting rate in seconds (0 = off)

10.1.1 Cycling Commands

The cycling mode alternates the filament current between two setpoints (P1 and P2) for a programmable number of cycles, used for cathode conditioning or bake-out sequences.

Command	Parameters	Description
SFLP1	<ch>,<A>	Sets cycle current 1 (first half of cycle)
GFLP1	<ch>	Returns cycle current 1
SFLP2	<ch>,<A>	Sets cycle current 2 (second half of cycle)
GFLP2	<ch>	Returns cycle current 2
SFLCY	<ch>,<n>	Sets cycle count (0 = run forever)
GFLCY	<ch>	Returns cycle count

SFLENAR	<ch>,<ON|OFF>	Starts/stops cycling mode
GFLENAR	<ch>	Returns cycling status (OFF or cycles remaining)

11 Analog Input Module

The Analog Input module is based on the Adafruit ADS1115 16-bit ADC. Up to 8 channels are supported (two ADS1115 devices). Channels can be read on demand or configured for high-speed vector recording.

11.1 Host Commands

Command	Parameters	Description
ADC	<ch>	Reads and reports ARM native ADC channel 0–3 (12-bit raw)
ADCINIT	—	Prepares ADC for vector acquisition; sets up buffer and triggers
ADCTRIG	—	Software trigger to start vector acquisition
ADCABORT	—	Aborts ongoing acquisition
SADCCHAN	<ch>	Selects acquisition channel (0–7)
GADCCHAN	—	Returns acquisition channel
SADCSAMPS	<n>	Sets samples per acquisition
GADCSAMPS	—	Returns samples per acquisition
SADCVECTS	<n>	Sets number of acquisition vectors
GADCVECTS	—	Returns vector count
SADCRATE	<Hz>	Sets sample rate (up to ~200 kHz per channel)
GADCRATE	—	Returns sample rate
ADCBPRO	<ch>	Reads and reports ADS1115 input; ch = 1–8
CDCBPRO	<ch>	Reports calibrated ADC value

12 Digital I/O

The MIPS controller provides digital inputs (Q–X, labelled on the rear panel) and digital outputs (A–H). These are 3.3 V / 5 V tolerant TTL logic signals. They can be read/written individually, triggered by conditions, or used to generate precision timing pulses.

12.1 Pin Commands

Command	Parameters	Description
SDIO	<pin>,<0|1>	Sets digital output pin state; pin = A–H
GDIO	<pin>	Returns digital pin state (input or output)
SDTRIGINP	<pin>,<POS|NEG>	Sets delayed-trigger input and active edge; pin = Q–X
SDTRIGDLY	<µs>	Sets trigger delay in microseconds
GDTRIGDLY	—	Returns trigger delay
SDTRIGPRD	<µs>	Sets trigger repeat period in µs
GDTRIGPRD	—	Returns repeat period
SDTRIGRPT	<n>	Sets number of trigger repeats (0 = forever)
GDTRIGRPT	—	Returns repeat count
SDTRIGMOD	<module>	Sets the module triggered by delayed trigger: ARB, ADC, SWEEP, AUXTRIG
SDTRIGENA	<TRUE|FALSE>	Enables/disables delayed trigger
GDTRIGENA	—	Returns delayed trigger enable state

12.2 Pulse Counter and Clock Generator

The clock generator produces pulses on the trigger output at a programmed frequency and width. The BURST command generates a fixed number of pulses.

Command	Parameters	Description
SWIDTH	<µs>	Sets trigger output pulse width in microseconds
GWIDTH	—	Returns pulse width
SFREQ	<Hz>	Sets trigger output frequency in Hz
GFREQ	—	Returns frequency
BURST	<n>	Generates n pulses on trigger output; n = −1 runs forever; n = 0 stops
TRIGOUT	<mode>	Controls trigger output mode: WIDTH (single pulse), FOLLOW (mirrors input S), FOLLOWS (debounced follow)

12.3 Pulse Sequence Generator

The Pulse Sequence Generator (PSG) provides programmable pulse patterns on one output channel. Parameters include period, width, delays, return timing, and gate arming.

Command	Parameters	Description
SPGENA	<TRUE|FALSE>	Enables/disables pulse sequence generator
GPGENA	—	Returns PSG enable state
SPGPER	<µs>	Sets PSG period in µs
GPGPER	—	Returns period
SPGWDTH	<µs>	Sets pulse width in µs
GPGWDTH	—	Returns width
SPGDLY	<µs>	Sets pulse delay in µs
GPGDLY	—	Returns delay
SPGRET	<µs>	Sets return time in µs
GPGRET	—	Returns return time
SPGNUM	<n>	Sets number of pulses per burst
GPGNUM	—	Returns pulse count
SPGOUTCH	<ch>	Sets output channel (A–H)
GPGOUTCH	—	Returns output channel
SPGTRG	<input>	Sets trigger input (Q–X or SW for software)
GPGTRG	—	Returns trigger input
SPGTRGF	<POS|NEG>	Sets trigger active edge
GPGTRGF	—	Returns trigger edge
SPGTRGL	<level>	Sets trigger level
GPGTRGL	—	Returns trigger level
SPGTRGO	<mode>	Sets trigger output mode
GPGTRGO	—	Returns trigger output mode
SPGARML	<level>	Sets arm level
GPGARML	—	Returns arm level
SPGARMT	<µs>	Sets arm timeout in µs
GPGARMT	—	Returns arm timeout
SPGSKIP	<n>	Sets skip count between pulses
GPGSKIP	—	Returns skip count
SPGPV	<V>	Sets pulse voltage
GPGPV	—	Returns pulse voltage

13 Pulse Sequence Tables

The table system is the most powerful feature of MIPS. A table defines a timed sequence of module events (voltage changes, digital output changes, triggers) that execute with microsecond precision under hardware timer control.

13.1 Table Syntax Overview

A table is defined by the STBLDAT command followed by a specially formatted string enclosed in semicolons. The full syntax is documented in Appendix C.

```
STBLDAT;0:[ch:mod,val,time:ch:mod2,val2,...];
```

Key concepts:

- Time points are in microseconds; minimum 9 µs (fast table mode)
- Multiple tables (0–15) can be pre-loaded and selected with STBLNUM
- Tables can be nested and looped
- Trigger sources: internal clock (INT), external (EXT), software (SW)

13.2 Table Management Commands

Command	Parameters	Description
STBLDAT	<table string>	Loads a pulse sequence table; see Appendix C for syntax
STBLCLK	<INT|EXT>	Sets table clock source
STBLTRG	<SW|EXT>	Sets table trigger mode
TBLSTRT	—	Issues a software table trigger
TBLSTOP	—	Stops a running table immediately
TBLABRT	—	Aborts table operation
SMOD	<mode>	Sets table looping mode: LOOP (continuous), ONCE (single run)
GTBLFRQ	—	Returns current internal table clock frequency
STBLNUM	<n>	Sets active table number (0–15)
GTBLNUM	—	Returns active table number
STBLADV	<ON|OFF>	Enables auto-advance to next table after completion
GTBLADV	—	Returns auto-advance state
STBLVLT	<tp>,<ch>,<V>	Sets a voltage value at time point tp, channel ch in the loaded table (live modification)
GTBLVLT	<tp>,<ch>	Returns the voltage value at a table entry
STBLCNT	<tp>,<ch>,<n>	Sets the repeat count at a table time point
STBLDLY	<ms>	Sets inter-table delay in milliseconds (default 4 ms)
SOFTLDAC	<TRUE|FALSE>	Forces software LDAC for DC bias table updates
GTBLREPLY	—	Returns table response enable state
STBLREPLY	<TRUE|FALSE>	Enables/disables table status response messages

TBLRPT	<n>	Reports loaded table n as hex bytes
TBLTSKENA	<TRUE|FALSE>	Enables background tasks during table execution
STBLRBT	<TRUE|FALSE>	Sets Twave readback test enable during tables

14 Level Detection Module (LDM)

The Level Detection Module (LDM) monitors an analogue input and triggers actions when a threshold is crossed. It is primarily used to adapt ARB alternate-waveform delay and duration in real time based on measured ion signal.

14.1 LDM Commands

Command	Parameters	Description
SDACV	<ch>,<V>	Sets named DAC channel voltage; ch = channel name string
GDACV	<ch>	Returns DAC channel voltage
SDACMAX	<ch>,<V>	Sets DAC channel maximum voltage limit
GDACMAX	<ch>	Returns maximum limit
SDACMIN	<ch>,<V>	Sets DAC channel minimum voltage limit
GDACMIN	<ch>	Returns minimum limit
SDACUN	<ch>,<units>	Sets DAC channel units string
GDACUN	<ch>	Returns units string
SDACNM	<mod>,<ch>,<name>	Sets DAC channel name by module number and channel index
GDACMN	<mod>,<ch>	Returns DAC channel name
GHVV	<ch>	Returns HVPS output voltage (also applicable to LDM HVPS sub-system)
GHVI	<ch>	Returns HVPS current
SHV	<ch>,<V>	Sets HVPS voltage
SHVDIS	<ch>	Disables HVPS channel
SHVENA	<ch>	Enables HVPS channel
SHVPSUP	<mod>,<V>	Sets HVPS positive supply
SHVNSUP	<mod>,<V>	Sets HVPS negative supply
CARBADLY	<addr>,<mask>	Configures LDM to control ARB alternate-waveform trigger delay; addr = hex TWI address of LDM (default 0x32); mask = hex ARB module bit mask (bits 0–5 correspond to modules 1–6)
CARBADUR	<addr>,<mask>	Configures LDM to control ARB alternate-waveform duration

15 ARB / Twave ARB Module

The ARB module generates arbitrary waveforms on 8 simultaneous output channels using 8-bit DACs at up to 1 MHz update rate (all channels). Up to 6 modules can be installed for 48 total outputs. Two modes are supported: TWAVE mode generates phase-shifted traveling waves; ARB mode provides general arbitrary waveform generation with trigger/burst capability.

15.1 Specifications

Output channels	8 per module (D15 male connector on MIPS rear panel)
Voltage range	±50 V (programmable offset), 0–100 Vp-p amplitude
DAC resolution	8-bit main; 12-bit offset and auxiliary
Max update rate	1 MHz (all 8 channels simultaneous)
Max frequency (TWAVE)	1.28 MHz ÷ PPP (default PPP=32 → 40 kHz)
Buffer length (ARB)	100–8000 samples
Auxiliary output	1 × BNC, ±50 V, 12-bit
Float input	1 × BNC; ground if unused (max 300 Vrms)
Max modules	6 per system (48 outputs total)
External clock	Optional clock in/out (0–5 V TTL)

15.2 Connections

- ARB channel outputs: D15 male connector, pins 1–8 are channels 1–8; pins 9–15 are ground
- Auxiliary output: BNC rear panel, ±50 V
- Float input: BNC rear panel; ground with shorting cap if unused
- Clock in/out (optional): 0–5 V TTL BNC; external clock max = 1.28 MHz

15.3 General Commands

Command	Parameters	Description
`SARBMODE`	<mod>,<TWAVE|ARB>	Sets operating mode for module mod
`GARBMODE`	<mod>	Returns operating mode
`SWFREQ`	<mod>,<Hz>	Sets waveform frequency in Hz
`GWFREQ`	<mod>	Returns frequency
`SWFVRNG`	<mod>,<Vpp>	Sets peak-to-peak output amplitude
`GWFVRNG`	<mod>	Returns amplitude

SWFVOFF	<mod>,<V>	Sets DC offset voltage (applied to all channels and aux)
GWFVOFF	<mod>	Returns DC offset
SWFVAUX	<mod>,<V>	Sets auxiliary output voltage (±50 V)
GWFVAUX	<mod>	Returns auxiliary voltage
SWFENA	<mod>	Enables waveform output for module mod
SWFDIS	<mod>	Disables waveform output
ARBSYNC	—	Issues software synchronisation pulse to all ARB modules
GARBVER	<mod>	Returns ARB module firmware version
GARBPPP	<mod>	Returns points-per-period (PPP) for Twave mode (default 32)
SARBPPP	<mod>,<PPP>	Sets PPP value (8–128); MIPS must be rebooted after change; affects max Twave frequency (max = 1.28 MHz ÷ PPP)
SARBEXT	<mod>,<MIPS|EXT>	Sets clock source when in common-clock mode: MIPS = controller clock; EXT = external BNC input
SWFVRAMP	<mod>,<V/s>	Sets voltage ramp rate in V/s; 0 = instant; applies to all 8 channels
GWFVRAMP	<mod>	Returns voltage ramp rate

15.3.1 TWAVE Mode Commands

Command	Parameters	Description
SWFDIR	<mod>,<FWD|REV>	Sets Twave direction; FWD = positive phase advance; REV = negative
GWFDIR	<mod>	Returns direction
SWFTYP	<mod>,<type>	Sets waveform type: SIN, RAMP, TRI, PULSE, ARB
GWFTYP	<mod>	Returns waveform type
SWFARB	<mod>,<v1,v2,...,v32>	Defines 32 custom waveform points (−100 to 100 % of peak)
GWFARB	<mod>	Returns custom waveform as 32 comma-separated values
SARBOFFA	<mod>,<V>	Sets output set-A offset (dual-board modules only); ±10 V
GARBOFFA	<mod>	Returns set-A offset
SARBOFFB	<mod>,<V>	Sets output set-B offset (dual-board modules only); ±10 V
GARBOFFB	<mod>	Returns set-B offset
SARBREVA	<mod>,<V>	Sets auxiliary output voltage to apply when direction = REV
CLRARBRV	<mod>	Clears the reverse-direction aux voltage; aux will not change when direction reverses

15.3.2 ARB Buffer Mode Commands

Command	Parameters	Description
SARBBUF	<mod>,<n>	Sets buffer length (100–8000 samples)
GARBBUF	<mod>	Returns buffer length
SARBNUM	<mod>,<n>	Sets repeat count per trigger (0 = forever)
GARBNUM	<mod>	Returns repeat count
SARBCHS	<mod>,<pct>	Sets all channels in the buffer to a uniform value (−100 to 100 %)
SARBCH	<mod>,<ch>,<pct>	Sets a single channel in the entire buffer; ch = 1–8
SACHRNG	<mod>,<ch>,<start>,<stop>,<pct>	Sets a channel within a buffer range to pct value
SARBSINE	<mod>,<ch>,<Hz>,<Vmin>,<Vmax>	Fills buffer channel ch with a sine wave at Hz between Vmin and Vmax

15.4 Alternate Waveform

The alternate waveform feature (requires ARB firmware 2.1+) allows switching from the primary Twave output to an alternate waveform state. Switching can be triggered by a host command, a digital input level, or a rising/falling edge with programmable delay and duration.

> **ℹ NOTE**
> All ARB modules share one hardware trigger/gate line for alternate waveform control. Configure only one module's SALTTRG; each module can individually enable or disable hardware use via SALTHWD.

Alternate waveform types (set with SALTWFM):

Type	Description
COMP	Default. Holds the final value of the last primary waveform cycle (compression waveform)
REV	Reverses the phase shift direction; same amplitude as primary
ARB	Applies the user-defined arbitrary waveform (SWFARB)
FIX	Applies user-defined fixed voltages on each of the 8 channels (set per-channel with SALTFVAL)
CUR	Applies the current primary waveform (use to change amplitude only; requires ARB FW 2.21 + MIPS FW 1.227)

Command	Parameters	Description
SALTENA	<mod>,<TRUE|FALSE>	Enables/disables alternate waveform for module mod
GALTENA	<mod>	Returns enable state
SALTWFM	<mod>,<type>	Sets alternate waveform type: COMP, REV, ARB, FIX, CUR
GALTWFM	<mod>	Returns alternate waveform type

SALTFVAL	<mod>,<ch>,<pct>	Sets the fixed-voltage value for channel ch (0–7) in FIX mode; −100 to 100 % of peak range
GALTFVAL	<mod>,<ch>	Returns fixed-voltage value for the channel
SALTTRG	<mod>,<Q-W|NA>	Selects digital input for alternate waveform trigger/gate (shared across all modules); NA disables
GALTTRG	<mod>	Returns configured trigger input
SALTHWD	<mod>,<TRUE|FALSE>	Enables this module's use of the hardware trigger/gate signal; must be TRUE for external trigger to work
GALTHWD	<mod>	Returns hardware trigger enable state
SALTTMODE	<mod>,<LEVEL|POS|NEG>	Sets trigger mode: LEVEL = alternate active while input is high; POS/NEG = edge triggered with delay/duration
GALTTMODE	<mod>	Returns trigger mode
SALTDLY	<mod>,<ms>	Sets delay from trigger edge to alternate waveform application (edge modes only)
GALTDLY	<mod>	Returns delay
SALTPLY	<mod>,<ms>	Sets duration for alternate waveform application after edge trigger
GALTPLY	<mod>	Returns duration
SALTRENA	<mod>,<TRUE|FALSE>	Enables use of separate amplitude for alternate waveform
GALTRENA	<mod>	Returns alternate amplitude enable state
SALTRNG	<mod>,<Vpp>	Sets alternate waveform amplitude in Vp-p
GALTRNG	<mod>	Returns alternate amplitude
SARBHISR	<mod>,<TRUE|FALSE>	Enables interrupt-service-routine processing of compression hardware signal (factory setting)
SARBCMPLN	<mod>,<1|2>	Selects hardware compression control line (1 or 2); default 2 (factory setting)
SARBSYNLN	<mod>,<1|2>	Selects hardware sync line (1 or 2); default 1 (factory setting)
SARBCPEX	<mod>,<TRUE|FALSE>	Enables compression hardware control line (factory setting)

15.4.1 Alternate Waveform Examples

Example 1: Command-controlled alternate waveform

```
SALTWFM,1,ARB        ; use custom ARB as alternate waveform
SALTHWD,1,FALSE      ; no hardware trigger
SALTRENA,1,TRUE      ; enable separate amplitude
SALTRNG,1,15         ; alternate amplitude = 15 Vp-p
SALTENA,1,TRUE       ; switch to alternate waveform
SALTENA,1,FALSE      ; return to primary waveform
```

Example 2: Level-triggered alternate waveform on input R

```
SARBHISR,1,TRUE      ; use ISR for compression signal
SARBCMPLN,1,2        ; use hardware line 2
SALTRENA,1,TRUE      ; enable alternate amplitude
```

```
SALTRNG,1,15
SALTWFM,1,ARB
SALTTRG,1,R          ; use digital input R
SALTHWD,1,TRUE       ; enable hardware trigger
SALTTMODE,1,LEVEL    ; active while R is high
```

Example 3: Edge-triggered with delay and duration

```
SALTTRG,1,R
SALTHWD,1,TRUE
SALTTMODE,1,POS      ; trigger on rising edge
SALTDLY,1,1.5        ; 1.5 ms delay after trigger
SALTPLY,1,3.5        ; apply for 3.5 ms
```

15.5 Compressor Commands (Two-Module TWAVE)

The ARB compressor uses the same parameters as the Twave compressor but references ARB modules. Module 2 is always the compression module.

Command	Parameters	Description
SARBCMODE	<Normal|Compress>	Sets ARB compressor mode
GARBCMODE	—	Returns compressor mode
SARBCORDER	<n>	Sets compression order
GARBCORDER	—	Returns compression order
SARBCTBL	<table>	Sets compressor multi-pass table
GARBCTBL	—	Returns table
SARBCTD	<ms>	Sets trigger delay
GARBCTD	—	Returns trigger delay
SARBCTC	<ms>	Sets compressed time
GARBCTC	—	Returns compressed time
SARBCTN	<ms>	Sets normal time
GARBCTN	—	Returns normal time
SARBCTNC	<ms>	Sets non-compressed time
GARBCTNC	—	Returns non-compressed time
TARBTRG	—	Forces a manual compressor trigger
SARBCSW	<Open|Close>	Sets compressor ion switch state
GARBCSW	—	Returns switch state
SARBCCLK	<mod>,<TRUE|FALSE>	Enables common clock for module mod
SARBCMP	<TRUE|FALSE>	Enables ARB compressor mode overall
SARBCOFF	<TRUE|FALSE>	Enables common offset for all ARB modules

15.6 ARB Sweep Commands

Frequency and amplitude sweeps can be driven by the MIPS controller (modules 1 and 2 only) or by the ARB module's own processor (any module). ARB-based sweeps support much faster rates.

Command	Parameters	Description
STWSSTRT	<mod>,<Hz>	Sets sweep start frequency
GTWSSTRT	<mod>	Returns start frequency
STWSSTP	<mod>,<Hz>	Sets sweep stop frequency
GTWSSTP	<mod>	Returns stop frequency
STWSSTRTV	<mod>,<Vpp>	Sets sweep start amplitude
GTWSSTRTV	<mod>	Returns start amplitude
STWSSTPV	<mod>,<Vpp>	Sets sweep stop amplitude
GTWSSTPV	<mod>	Returns stop amplitude
STWSTM	<mod>,<sec>	Sets sweep time in seconds
GTWSTM	<mod>	Returns sweep time
STWSGO	<mod>	Starts MIPS-controlled sweep (mod=3 triggers both 1 and 2)
STWSHLT	<mod>	Stops MIPS-controlled sweep
GTWSTA	<mod>	Returns MIPS sweep status: IDLE, STARTING, SWEEPING, STOPPING
SARBSGO	<mod>	Starts ARB-module-controlled sweep
SARBSHLY	<mod>	Stops ARB-module sweep
GARBSTA	<mod>	Returns ARB sweep status: IDLE, STARTING, SWEEPING, STOPPING

15.7 System Configuration Commands

Command	Parameters	Description
SARBADD	<mod>,<addr>	Sets TWI address for module mod (base 10); factory setting
SARBDBRD	<mod>,<TRUE|FALSE>	Sets dual-output-board flag for module mod
SARBCCLK	<mod>,<TRUE|FALSE>	Enables common clock for module mod (uses MIPS or external clock)

16 FAIMS Module

> **⚠ WARNING**
> The FAIMS module generates RF voltages exceeding 5,000 V peak. Keep the RF deck fully enclosed during operation. Use the emergency OFF button on the RF deck to immediately disable RF.

The FAIMS module produces the asymmetric bisinusoidal high-voltage waveforms required for FAIMS/DMS ion filtering. The primary frequency is approximately 1 MHz and the harmonic is 2 MHz. Peak-to-peak output reaches 5,500 V. DC compensation voltage (CV), DC bias, and DC offset are independently adjustable.

16.1 Host Commands

Command	Parameters	Description
SFMENA	<TRUE|FALSE>	Enables FAIMS high-voltage waveform generation
GFMENA	—	Returns enable state
SFMDRV	<%>	Sets RF drive level in percent (0–100)
GFMDRV	—	Returns drive level
GFMPWR	—	Returns total RF power in watts
GFMPV	—	Returns positive peak output voltage in kV
GFMNV	—	Returns negative peak output voltage in kV
SFMCV	<V>	Sets DC compensation voltage (CV) setpoint
GFMCV	—	Returns CV setpoint
GFMCVA	—	Returns actual CV readback voltage
SFMBIAS	<V>	Sets DC bias voltage setpoint
GFMBIAS	—	Returns bias setpoint
GFMBIASA	—	Returns actual bias readback
SFMOFF	<V>	Sets DC offset voltage
GFMOFF	—	Returns offset setpoint
GFMOFFA	—	Returns actual offset readback
SRFHPCAL	<mod>,<V>	Sets positive harmonic peak readback calibration
SRFHNCAL	<mod>,<V>	Sets negative harmonic peak readback calibration
SARCDIS	<TRUE|FALSE>	Disables arc detection when TRUE (use with caution)
SFMATBPC	<V>	Sets auto bias pickup calibration voltage
GFMATBPC	—	Returns auto bias pickup calibration
SFMCCUR	<A>	Sets compensation current
GFMCCUR	—	Returns compensation current
SFMMDIS	<TRUE|FALSE>	Sets FAIMS monitor disable flag
GFMMDIS	—	Returns monitor disable state
SFMSTPTM	<ms>	Sets stop time for CV scan
GFMSTPTM	—	Returns stop time

SFMSTRTLIN	<V>	Sets CV scan start line voltage
GFMSTRTLIN	—	Returns scan start voltage
SFMSTRTSTP	<V>	Sets CV scan start-stop voltage
GFMSTRTSTP	—	Returns scan start-stop
SFMTPOS	<V>	Sets CV target position
GFMTPOS	—	Returns target position
SFMUSEPWL	<TRUE|FALSE>	Enables piecewise linear CV calibration
GFMUSEPWL	—	Returns PWL calibration state

17 FAIMS Variants: FAIMSfb and HOFAIMS

The FAIMSfb (Feedback) and HOFAIMS (High-Order FAIMS) are variants of the base FAIMS module with additional control channels and higher output capability respectively.

17.1 FAIMSfb Additional Commands

The FAIMSfb module adds feedback-controlled CV scanning. Commands controlling the scan are issued directly to the FAIMSfb subsystem.

Command	Parameters	Description
GRPCYC	—	Returns repetition cycle count
SRPCYC	<n>	Sets repetition cycle count
GRPENA	—	Returns repetition enable state
SRPENA	<TRUE|FALSE>	Enables/disables repetition
GRPPER	<ms>	Returns repetition period in ms
SRPPER	<ms>	Sets repetition period
GRPTRG	—	Returns trigger input for repetition
SRPTRG	<input>	Sets trigger input
GRPTRGL	—	Returns trigger level
SRPTRGL	<level>	Sets trigger level
GRPDCBC	—	Returns DC bias channel configuration
SRPDCBC	<ch>	Sets DC bias channel for FAIMSfb control
GRPCHENA	—	Returns channel enable state
SRPCHENA	<ch>,<TRUE|FALSE>	Enables/disables FAIMSfb channel
GRAMP	—	Returns ramp parameters
SRAMP	<start>,<stop>,<step>,<dwell>	Sets CV ramp scan: start voltage, stop voltage, step size, dwell time per step (ms)
GRFALL	—	Returns fall-through ramp state
SRFALL	<TRUE|FALSE>	Sets fall-through ramp enable

17.2 HOFAIMS Additional Commands

HOFAIMS provides higher output voltages and independent control of two high-voltage channels. Commands follow the same naming convention as FAIMS but address both positive and negative supplies independently.

Refer to the MIPS FAIMS Rev 3.0 addendum for complete HOFAIMS command reference. The HOFAIMS module responds to most standard FAIMS commands and adds the following:

- Independent positive and negative HV supply control
- Remote emergency-stop input on digital input S (active high)
- Power and drive limits configurable via firmware

18 RF QUAD Module

The RF QUAD module provides quadrupole mass filter control, combining the RF ion guide driver with a resolving DC system. It accepts m/z and resolution parameters and automatically calculates the required RF and DC voltages. Up to 2 QUAD modules can be installed.

18.1 Specifications

RF output	Up to 1,500 Vp-p (hardware dependent)
Frequency range	50 kHz – 5 MHz
Resolving DC	Supplied via DC bias channels 1 and 2 (configurable with SRFADCCH)
Pole bias	Independent DC supply on each pole; configurable
m/z scan	Automated m/z scan using SRFAMZ and RFAQUPDATE
Auto-tune	Two-phase: frequency scan at low drive, then RF/SWR optimisation at high drive
Max modules	2 per system

18.2 Host Commands

Command	Parameters	Description
SRFAFRQ	<mod>,<Hz>	Sets QUAD RF frequency in Hz
GRFAFRQ	<mod>	Returns RF frequency
SRFADRV	<mod>,<%>	Sets RF drive level in percent
GRFADRV	<mod>	Returns drive level
SRFAVLT	<mod>,<V>	Sets RF output voltage setpoint (auto mode)
GRFAVLT	<mod>	Returns voltage setpoint
GRFAPPVP	<mod>	Returns positive peak RF voltage readback
GRFAPPVN	<mod>	Returns negative peak RF voltage readback
GRFAFPWR	<mod>	Returns RF amplifier forward power in watts
SRFARNG	<mod>,<Vpp>	Sets maximum RF level (factory configuration)
GRFARNG	<mod>	Returns maximum RF level
SRFAPB	<mod>,<V>	Sets pole bias DC voltage in volts
GRFAPB	<mod>	Returns pole bias voltage
SRFARDC	<mod>,<V>	Sets resolving DC ± voltages (applied to DC bias channels 1 and 2)
GRFARDC	<mod>	Returns resolving DC setting
SRFAR0	<mod>,<mm>	Sets Ro (inscribed radius) in mm
GRFAR0	<mod>	Returns Ro
SRFAMZ	<mod>,<m/z>	Sets target m/z in amu

GRFAMZ	<mod>	Returns m/z
SRFARES	<mod>,<AMU>	Sets resolution in AMU
GRFARES	<mod>	Returns resolution
RFAQUPDATE	<mod>	Recalculates and applies RF and DC voltages based on Ro, m/z, and resolution
SRFAGAIN	<mod>,<HIGH|LOW>	Sets RF level control gain: HIGH or LOW
GRFAGAIN	<mod>	Returns gain setting
RRFAAMP	<mod>	Reports full RF amplifier parameter set
SRFADCCH	<mod>,<ch>	Sets DC bias channel used for resolving DC; ch=1 means channel 1 for pole 1, channel 2 for pole 2
GRFADCCH	<mod>	Returns resolving DC channel assignment
SRDCENA	<TRUE|FALSE>	Enables/disables resolving DC output
GRDCENA	—	Returns resolving DC enable state
SRFAAR	<mod>,<TRUE|FALSE>	Enables automatic level range selection
GRFAAR	<mod>	Returns automatic range state
SRFACP	<mod>,<TRUE|FALSE>	Enables frequency compensation algorithm
GRFACP	<mod>	Returns frequency compensation state
SRFACPF	<mod>,<Hz>	Sets base frequency for compensation (calibration reference)
GRFACPF	<mod>	Returns base frequency
SRFACPG	<mod>,<gain>	Sets frequency compensation gain factor; correction = (actual_freq − base_freq) × gain; adjusts level control to compensate frequency-dependent RF level changes
GRFACPG	<mod>	Returns compensation gain
SRFDRVZ	<mod>,<zp>	Sets RF drive level that produces zero RF output (hardware offset calibration)

18.3 Auto-Tune

The auto-tune system scans frequency to find the resonance peak then optimises the drive. Two phases are used: Phase 1 scans frequency at a moderate drive level to locate the peak; Phase 2 increases drive and either maximises RF output level or minimises SWR.

> **ℹ NOTE**
> Auto-tune parameters (SRFATMINF, SRFATMAXF, SRFATHP, SRFATSWR) apply to all QUAD modules and are not saved to EEPROM. Reconfigure after each reboot if needed.

Command	Parameters	Description
SRFATUNE	<mod>	Starts auto-tune for the selected QUAD module
SRFATUNER	<mod>	Starts auto-tune and reports detailed results to console
SRFATMINF	<Hz>	Sets minimum frequency for the auto-tune scan
GRFATMINF	—	Returns auto-tune minimum frequency
SRFATMAXF	<Hz>	Sets maximum frequency for the auto-tune scan

GRFATMAXF	—	Returns auto-tune maximum frequency
SRFATHP	<%>	Sets the Phase 2 drive level as a percentage of full drive
GRFATHP	—	Returns Phase 2 drive level
SRFATSWR	<TRUE|FALSE>	TRUE = Phase 2 minimises SWR; FALSE = Phase 2 maximises RF level
GRFATSWR	—	Returns Phase 2 tuning objective (TRUE = SWR, FALSE = level)

18.4 Mass Calibration

The QUAD system's output voltages are factory-calibrated for the RF levels, but mass calibration in your specific system requires further adjustment. Use a known single-mass standard and the following procedure:

6. Set Ro to the mechanical inscribed radius of the quadrupole rods (in mm).
7. Set target m/z using SRFAMZ.
8. Set resolution using SRFARES.
9. Issue RFAQUPDATE to apply calculated voltages.
10. Monitor the ion signal while adjusting Ro or the DC bias calibration until the expected mass window is centred.

19 States and Segments

The States and Segments system provides a high-level sequencing capability for DC bias profiles. A State is a named set of DC bias setpoints; Segments define time-based transitions between States.

Command	Parameters	Description
GSTATE	<name>	Returns the voltage configuration for named state
SSTATE	<name>,<voltages>	Sets DC bias values for named state
TSEGMENT	—	Triggers start of a segment sequence
DSEGMENT	<n>	Displays segment n parameters
ADDSEGTP	<n>,<tp>	Adds a time point to segment n
ADDSEGSTRG	<n>,<string>	Adds command string to segment n
ADDSEGTRG	<n>,<trigger>	Adds a trigger condition to segment n
DSTATE	<name>	Deletes named state
GPSWD	—	Returns password setting
SPSWD	<pwd>	Sets password

Appendix A Complete Command Reference by Module

This appendix provides a compact one-line summary of all MIPS host commands grouped by module. For detailed descriptions including parameter ranges, see the corresponding chapter.

A.1 General System Commands

Command	Parameters	Description
GVER	—	Firmware version string
GERR	—	Last error code
GNAME	—	System name
SNAME	<name>	Set system name
UUID	—	128-bit unique ID (hex)
ABOUT	—	System summary
SMREV	<b>,<a>,<r>	Set module revision
RESET	—	Software reboot
STATUS	—	Reboot reason + uptime ms
SAVE	—	Save config to SD
GCHAN	<sys>	Number of channels for system
MUTE	<T|F>	Suppress ACK/NAK
ECHO	<T|F>	Echo commands
TRIGOUT	<mode>	Trigger output control
DELAY	<ms>	Insert delay
GCMDS	—	List all commands
GAENA/SAENA	<T|F>	Analog input enable
THREADS	—	List threads
STHRDENA	<n>,<T|F>	Enable/disable thread
SDEVADD	<b>,<a>	Define device address
SSPND/GSPND	<T|F>	Task suspend
CPUTEMP	—	CPU temperature °C
TWITALK	<b>,<a>	Redirect serial to TWI device
LEDOVRD	<T|F>	Override LED
LED	<mask>	Set LED state
DSPOFF	<T|F>	Disable display
SSERIALNAV	<T|F>	Enable serial UI navigation
TRACE	—	Enable trace buffer
TBLTSKENA	<T|F>	Enable tasks in table mode
SOFTLDAC	<T|F>	Force software LDAC
BIMAGE	<file>	Set boot image
CHKIMAGE	<file>	Check image file

LOADIMAGE	<file>	Load image to display
DIR	—	List SD files
DEL	<file>	Delete SD file
GET	<file>	Dump SD file as hex
PUT	<file>,<sz>	Write hex data to SD file
SAVEMOD	<f>,<b>,<a>	Save module EEPROM to SD
LOADMOD	<f>,<b>,<a>	Load module EEPROM from SD
SAVEALL	—	Save all module EEPROMs
LOADALL	—	Load all module EEPROMs
GETEEPROM	<b>,<a>	Send EEPROM to host
PUTEEPROM	<b>,<a>	Write EEPROM from host
MRECORD	<file>	Start macro recording
MSTOP	—	Stop macro recording
MPLAY	<file>	Play macro
MLIST	—	List macros
MDELETE	<file>	Delete macro

A.2 Wi-Fi and Ethernet

Command	Parameters	Description
GHOST/SHOST	<name>	Wi-Fi host name
GSSID/SSSID	<ssid>	Wi-Fi SSID
GPSWD/SPSWD	<pwd>	Wi-Fi password
SWIFIENA	<T|F>	Enable Wi-Fi at next reboot
SWIFISP	<0|1>	Wi-Fi UART port selection
GEIP/SEIP	<ip>	Ethernet IP address
GESNIP/SESNIP	<ip>	Ethernet subnet mask
GEPORT/SEPORT	<port>	Ethernet TCP port
GEGATE/SEGATE	<ip>	Ethernet gateway
ENTEST	—	Test Ethernet adapter

A.3 RF Driver

Command	Parameters	Description
SRFFRQ/GRFFRQ	<ch>,<Hz>	RF frequency
SRFDRV/GRFDRV	<ch>,<%>	RF drive level
SRFVLT/GRFVLT	<ch>,<V>	RF voltage setpoint (auto)
GRFPPVP/GRFPPVN	<ch>	Peak voltage readbacks
GRFPWR	<ch>	RF power (W)

SRFMODE/GRFMODE	<ch>,<mode>	Mode: MANUAL, AUTO
SRFATUNE	<ch>	Auto-tune
SRFRETUNE	<ch>	Retune (fine)
SRFCAL	<ch>,<V>,<V>	Calibration
SRFHPCAL/SRFHNCAL	<ch>,<V>	Harmonic calibration
SEGATE/GEGATE	<ch>,<in>	Gate input selection

A.4 DC Bias

Command	Parameters	Description
SDCB/GDCB	<ch>,<V>	Voltage setpoint
GDCBV	<ch>	Readback voltage
SDCBOF/GDCBOF	<b>,<V>	Float voltage
GDCMIN/GDCMAX	<ch>	Min/max voltage
SDCPWR/GDCPWR	<ON|OFF>	Power supply
SDCBALL/GDCBALL	<V1,...>	All channels set/report
GDCBALLV	—	All readback voltages
SDCBDELTA	<ΔV>	Adjust all by delta
SDCBPRO/GDCBPRO	<n>,<...>	Voltage profile
ADCBPRO	<n>	Apply profile
CDCBPRO	<n>	Copy current to profile
TDCBPRO	<n1>,<n2>,<ms>	Toggle profiles
TDCBSTP	—	Stop toggle
SDCBPV/GDCBPV	<ch>,<V>	Pulse voltage
SDCBPW/GDCBPW	<ch>,<µs>	Pulse width
SDCBPT/GDCBPT	<ch>,<µs>	Pulse period
SDCBPD/GDCBPD	<ch>,<µs>	Pulse delay
SDCBPENA/GDCBPENA	<ch>,<T|F>	Enable pulse mode
SDCBPCH/GDCBPCH	<ch>,<n>	Pulse count
SDCBTEST	<T|F>	Enable readback testing
SDCBARST	<T|F>	Auto-reset on trip
DCBOFFRBENA	<T|F>	Enable offset readback
SDCBONEOFF	<T|F>	Single offset DAC
SDCBCHNS	<b>,<n>	Board channel count
SDCBRNG	<b>,<r>	Board voltage range

A.5 ESI

Command	Parameters	Description

SHV/GHV	<ch>,<V>	HV voltage setpoint
GHVV	<ch>	HV readback
GHVI	<ch>	Current readback (µA)
SHVENA/SHVDIS	<ch>	Enable/disable HV
GHVSTATUS	<ch>	ESI status
SHVPSUP/SHVNSUP	<m>,<V>	Positive/negative supply
GHVMAX/GHVMIN	<ch>	Voltage limits
GHVITST/SHVITST	<T|F>	Current test enable

A.6 Twave

Command	Parameters	Description
STWF/GTWF	<m>,<Hz>	Frequency
STWPV/GTWPV	<m>,<V>	Pulse voltage
STWG1V/GTWG1V	<m>,<V>	Guard 1 voltage
STWG2V/GTWG2V	<m>,<V>	Guard 2 voltage
STWSEQ/GTWSEQ	<m>,<seq>	Sequence string
STWDIR/GTWDIR	<m>,<dir>	Direction FWD/REV
STWCMODE/GTWCMODE	<mode>	Compressor mode
STWCORDER/GTWCORDER	<n>	Compression order
STWCTBL/GTWCTBL	<table>	Compressor table
STWCTD/GTWCTD	<ms>	Trigger delay
STWCTC/GTWCTC	<ms>	Compressed time
STWCTN/GTWCTN	<ms>	Normal time
STWCTNC/GTWCTNC	<ms>	Non-compressed time
TWCTRG	—	Manual trigger
STWCSW/GTWCSW	<O|C>	Switch state
STWCCLK/STWCMP	<T|F>	Common clock / compressor enable
STWSSTRT/GTWSSTRT	<m>,<Hz>	Sweep start frequency
STWSSTP/GTWSSTP	<m>,<Hz>	Sweep stop frequency
STWSSTRTV/GTWSSTRTV	<m>,<V>	Sweep start voltage
STWSSTPV/GTWSSTPV	<m>,<V>	Sweep stop voltage
STWSTM/GTWSTM	<m>,<s>	Sweep time
STWSGO/STWSHLT	<m>	Start/stop sweep
GTWSTA	<m>	Sweep status

A.7 ARB Module

Command	Parameters	Description

SARBMODE/GARBMODE	<m>,<mode>	Operating mode TWAVE/ARB
SWFREQ/GWFREQ	<m>,<Hz>	Frequency
SWFVRNG/GWFVRNG	<m>,<Vpp>	Amplitude
SWFVOFF/GWFVOFF	<m>,<V>	DC offset
SWFVAUX/GWFVAUX	<m>,<V>	Aux output voltage
SWFENA/SWFDIS	<m>	Start/stop output
SWFTYP/GWFTYP	<m>,<type>	Waveform type
SWFDIR/GWFDIR	<m>,<dir>	Direction FWD/REV
SWFARB/GWFARB	<m>,<pts>	Custom waveform (32 points)
SWFVRAMP/GWFVRAMP	<m>,<V/s>	Voltage ramp rate
ARBSYNC	—	Sync all modules
GARBVER	<m>	ARB firmware version
GARBPPP/SARBPPP	<m>[,<n>]	Points per period (Twave)
SARBEXT	<m>,<MIPS|EXT>	Clock source
SARBBUF/GARBBUF	<m>,<n>	Buffer length (ARB mode)
SARBNUM/GARBNUM	<m>,<n>	Buffer repeat count
SARBCHS	<m>,<pct>	Initialize all channels
SARBCH	<m>,<ch>,<pct>	Set one channel
SACHRNG	<m>,<ch>,<s>,<e>,<pct>	Set channel range
SARBOFFA/GARBOFFA	<m>,<V>	Set-A offset (dual-board)
SARBOFFB/GARBOFFB	<m>,<V>	Set-B offset
SARBREVA	<m>,<V>	Aux voltage in REV direction
CLRARBRV	<m>	Clear REV aux voltage
SALTENA/GALTENA	<m>,<T|F>	Alternate waveform enable
SALTWFM/GALTWFM	<m>,<type>	Alt waveform type
SALTFVAL/GALTFVAL	<m>,<ch>,<pct>	FIX mode per-channel value
SALTTRG/GALTTRG	<m>,<in>	Alt trigger input
SALTHWD/GALTHWD	<m>,<T|F>	Hardware trigger enable
SALTTMODE/GALTTMODE	<m>,<mode>	Trigger mode LEVEL/POS/NEG
SALTDLY/GALTDLY	<m>,<ms>	Trigger delay
SALTPLY/GALTPLY	<m>,<ms>	Alt waveform duration
SALTRENA/GALTRENA	<m>,<T|F>	Alternate amplitude enable
SALTRNG/GALTRNG	<m>,<Vpp>	Alternate amplitude
SARBCCLK	<m>,<T|F>	Common clock enable
SARBCMP	<T|F>	Compressor enable
SARBCOFF	<T|F>	Common offset enable
SARBCTBL/GARBCTBL	<table>	Compressor table
SARBCMODE/GARBCMODE	<mode>	Compressor mode
SARBCORDER/GARBCORDER	<n>	Compression order
SARBCTD/GARBCTD	<ms>	Trigger delay

SARBCTC/GARBCTC	<ms>	Compressed time
SARBCTN/GARBCTN	<ms>	Normal time
SARBCTNC/GARBCTNC	<ms>	Non-compressed time
TARBTRG	—	Manual trigger
SARBCSW/GARBCSW	<O|C>	Ion switch
STWSSTRT/GTWSSTRT	<m>,<Hz>	Sweep start freq
STWSSTP/GTWSSTP	<m>,<Hz>	Sweep stop freq
STWSSTRTV/GTWSSTRTV	<m>,<V>	Sweep start Vpp
STWSSTPV/GTWSSTPV	<m>,<V>	Sweep stop Vpp
STWSTM/GTWSTM	<m>,<s>	Sweep time
STWSGO/STWSHLT	<m>	Start/stop MIPS sweep
GTWSTA	<m>	MIPS sweep status
SARBSGO	<m>	Start ARB sweep
SARBSHLY	<m>	Stop ARB sweep
GARBSTA	<m>	ARB sweep status
CARBADLY	<addr>,<mask>	LDM-controlled delay
CARBADUR	<addr>,<mask>	LDM-controlled duration

A.8 Filament

Command	Parameters	Description
SFLI/GFLI	<ch>,<A>	Current setpoint
GFLAI	<ch>	Actual current
SFLSV/GFLSV	<ch>,<V>	Supply voltage
GFLASV	<ch>	Actual supply voltage
GFLV	<ch>	Filament voltage
GFLPWR	<ch>	Power (W)
SFLENA/GFLENA	<ch>,<ON|OFF>	Enable
SFLRT/GFLRT	<ch>,<A/s>	Ramp rate
SFLDIR/GFLDIR	<ch>,<dir>	Current direction
SFLP1/GFLP1	<ch>,<A>	Cycle current 1
SFLP2/GFLP2	<ch>,<A>	Cycle current 2
SFLCY/GFLCY	<ch>,<n>	Cycle count
SFLENAR/GFLENAR	<ch>,<ON|OFF>	Cycling enable
SFLSRES/GFLSRES	<Ω>	Sense resistor value
GFLECUR	—	Emission current
SFLSWD	<T|F>	Serial watchdog
RFLPARMS	<ch>,<Hz>	Reporting rate

A.9 FAIMS

Command	Parameters	Description
SFMENA/GFMENA	<T|F>	Enable RF generation
SFMDRV/GFMDRV	<%>	Drive level
GFMPWR	—	Total power (W)
GFMPV/GFMNV	—	Peak voltages (kV)
SFMCV/GFMCV	<V>	CV setpoint
GFMCVA	—	CV actual
SFMBIAS/GFMBIAS	<V>	Bias setpoint
GFMBIASA	—	Bias actual
SFMOFF/GFMOFF	<V>	Offset setpoint
GFMOFFA	—	Offset actual
SRFHPCAL/SRFHNCAL	<m>,<V>	Harmonic calibration
SARCDIS	<T|F>	Arc detect disable
SFMATBPC/GFMATBPC	<V>	Auto bias pickup cal
SFMCCUR/GFMCCUR	<A>	Compensation current
SFMSTPTM/GFMSTPTM	<ms>	CV scan stop time
SFMSTRTLIN/GFMSTRTLIN	<V>	CV scan start voltage
SFMSTRTSTP/GFMSTRTSTP	<V>	CV scan start-stop
SFMTPOS/GFMTPOS	<V>	CV target position
SFMUSEPWL/GFMUSEPWL	<T|F>	Piecewise linear cal

A.10 RF QUAD

Command	Parameters	Description
SRFAFRQ/GRFAFRQ	<m>,<Hz>	RF frequency
SRFADRV/GRFADRV	<m>,<%>	Drive level
SRFAVLT/GRFAVLT	<m>,<V>	Voltage setpoint
GRFAPPVP/GRFAPPVN	<m>	Peak voltage readbacks
GRFAFPWR	<m>	Forward power (W)
SRFARNG/GRFARNG	<m>,<V>	Max RF level (factory)
SRFAPB/GRFAPB	<m>,<V>	Pole bias DC
SRFARDC/GRFARDC	<m>,<V>	Resolving DC ±
SRFAR0/GRFAR0	<m>,<mm>	Inscribed radius Ro
SRFAMZ/GRFAMZ	<m>,<m/z>	Target m/z
SRFARES/GRFARES	<m>,<AMU>	Resolution
RFAQUPDATE	<m>	Recalculate and apply voltages
SRFAGAIN/GRFAGAIN	<m>,<H|L>	Level control gain
RRFAAMP	<m>	Report amplifier parameters

SRFADCCH/GRFADCCH	<m>,<ch>	Resolving DC channel assignment
SRDCENA/GRDCENA	<T|F>	Resolving DC enable
SRFAAR/GRFAAR	<m>,<T|F>	Auto range
SRFACP/GRFACP	<m>,<T|F>	Frequency compensation enable
SRFACPF/GRFACPF	<m>,<Hz>	Compensation base frequency
SRFACPG/GRFACPG	<m>,<gain>	Compensation gain factor
SRFATUNE	<m>	Start auto-tune
SRFATUNER	<m>	Auto-tune with console report
SRFATMINF/GRFATMINF	<Hz>	Auto-tune min frequency
SRFATMAXF/GRFATMAXF	<Hz>	Auto-tune max frequency
SRFATHP/GRFATHP	<%>	Auto-tune Phase 2 drive
SRFATSWR/GRFATSWR	<T|F>	Phase 2: TRUE=minimise SWR; FALSE=maximise level
SRFDRVZ	<m>,<zp>	Drive zero-offset calibration

A.11 Digital I/O and Timing

Command	Parameters	Description
SDIO/GDIO	<pin>,[<0|1>]	Digital I/O pin state
SWIDTH/GWIDTH	[<µs>]	Trigger pulse width
SFREQ/GFREQ	[<Hz>]	Trigger frequency
BURST	<n>	Pulse burst
TRIGOUT	<mode>	Trigger output mode
SDTRIGINP	<pin>,<edge>	Delayed trigger input
SDTRIGDLY/GDTRIGDLY	[<µs>]	Trigger delay
SDTRIGPRD/GDTRIGPRD	[<µs>]	Trigger period
SDTRIGRPT/GDTRIGRPT	[<n>]	Trigger repeat count
SDTRIGMOD	<mod>	Trigger module
SDTRIGENA/GDTRIGENA	[<T|F>]	Trigger enable
ADC	<ch>	Read ADC channel
ADCINIT/ADCTRIG/ADCABORT	—	ADC vector acquisition
SADCCHAN/GADCCHAN	[<ch>]	ADC channel selection
SADCSAMPS/GADCSAMPS	[<n>]	ADC sample count
SADCVECTS/GADCVECTS	[<n>]	ADC vector count
SADCRATE/GADCRATE	[<Hz>]	ADC sample rate

A.12 Pulse Sequence Tables

Command	Parameters	Description
STBLDAT	<string>	Load table (see Appendix C)

STBLCLK	<INT|EXT>	Clock source
STBLTRG	<SW|EXT>	Trigger source
TBLSTRT	—	Software trigger
TBLSTOP	—	Stop table
TBLABRT	—	Abort table
SMOD	<LOOP|ONCE>	Loop mode
GTBLFRQ	—	Current clock frequency
STBLNUM/GTBLNUM	[<n>]	Active table number
STBLADV/GTBLADV	[<T|F>]	Auto-advance
STBLVLT	<tp>,<ch>,<V>	Modify voltage in loaded table
GTBLVLT	<tp>,<ch>	Read table entry voltage
STBLCNT	<tp>,<ch>,<n>	Modify repeat count
STBLDLY	<ms>	Inter-table delay
GTBLREPLY/STBLREPLY	[<T|F>]	Table response messages
TBLRPT	<n>	Report table as hex

Appendix B Error Codes

The GERR command returns the last error code. Error code 0 means no error. After reading, the code is retained until the next command that generates a new code.

Code	Meaning
0	No error
1	Bad argument — parameter out of range or wrong type
2	Module not found — addressed module not present
3	Bad board select — invalid board designation
4	TWI communications error
5	EEPROM read error
6	EEPROM write error
7	SD card error
8	File not found
9	Not implemented — command not supported by installed firmware
10	Bad index — array or table index out of bounds
11	Busy — command cannot execute while system is in current state
12	Over temperature
13	Voltage error — DC bias readback exceeds trip threshold
14	Current trip — ESI over-current
15	FAIMS arc detected

Appendix C Pulse Sequence Table Syntax Reference

This appendix provides a complete reference for the STBLDAT pulse sequence table language.

C.1 Overall Format

```
STBLDAT;<table_number>:[<time_us>:<entry>[:<entry>...],[<time_us>:<entry>...]],...;
```

- Table numbers: 0–15
- Time values are in whole microseconds; minimum 9 µs per time point
- Multiple entries at the same time point are separated by commas
- Tables end with a] character

C.2 Entry Format

```
<channel>:<module_code>:<value>
```

Field	Values	Description
channel	1–32	DC bias channel number (module × 8 + channel offset)
module_code	See C.3	Identifies which module type and operation
value	Module-specific	Voltage (V), percentage, or digital state

C.3 Module Codes

Code	Type	Description
1	DC Bias	DC bias module channel; value in volts
2	DC Bias	Second DC bias module channel
3	DC Bias	Third DC bias module channel
4	DC Bias	Fourth DC bias module channel
5–8	Digital	DIO output A–H; value 0 or 1
9	ESI	ESI voltage; value in volts
10–13	Twave	Twave module 1 and 2 parameters
14	RF Driver	RF output level; value in volts
15	ARB	ARB module channel; value in percent
16–27	ARB	ARB channels 1a–1h, 2a–2h per module
100–108	ARB Aux	ARB aux and offset channels (see firmware source)

t	Trigger out	Output trigger pulse; value = width in µs
b	Burst	Clock burst; value = number of pulses
c:A	ARB Comp	Trigger ARB compression table
c:T	Twave Comp	Trigger Twave compression table

C.4 Special Syntax

Syntax	Description
[n: ...]	Loop: execute contents n times (0 = loop forever)
[<nested>]	Nesting: tables can be nested up to 5 levels deep
R	Ramp mode: generates a linear voltage ramp between two time points
t<width>	Trigger pulse: output trigger for width µs
b<count>	Burst: generate count clock pulses on trigger output
0:[...	First time point; must start at time 0

C.5 Examples

Two-State Square Wave on DC Bias Ch 1 (±10 V, 100 µs period)

```
STBLDAT;0:[0:1:2:-10,100:1:2:10];
```

Voltage Ramp on DC Bias Ch 1 from 0 to 50 V over 1 ms with Digital Output A Pulse

```
STBLDAT;0:[0:1:2:0,0:5:2:1,1000:1:2:50R,1000:5:2:0];
```

Nested Loop — Repeat Inner 10 Times, Outer 3 Times

```
STBLDAT;0:[3:[0:1:2:-5,100:[10:1:2:5,200:1:2:-5]]];
```

C.6 Timing

Minimum time point spacing: 9 µs in fast table mode. The system pre-processes DAC data at load time, so only timing overhead at execution time is the DAC SPI transfer (~5–7 µs per channel). For best timing performance:

- Use TBLTSKENA,FALSE to disable background tasks during critical table sections
- Set STBLDLY to the minimum value (4 ms default) when chaining tables
- Use integer microsecond values; fractional µs not supported

Appendix D Quick-Start Guides

D.1 First Power-On

11. Connect the MIPS unit to mains power (100–240 VAC).
12. Insert a formatted micro-SD card (FAT32).
13. Power on; the display shows 'MIPS main menu' after module discovery.
14. Connect USB cable to host PC; a COM port appears within seconds.
15. Open a terminal (9600 baud settings are irrelevant for USB CDC; any settings work).
16. Type GVER and press Enter; the firmware version should appear.
17. Type ABOUT to list all discovered modules.
18. Type SAVE to create default.cfg on the SD card.

D.2 Setting DC Bias Channels

```
SDCPWR,ON            ; enable DC bias power supply
SDCB,1,50.0          ; set channel 1 to +50 V
SDCB,2,-25.0         ; set channel 2 to -25 V
GDCBALL              ; verify all setpoints
GDCBALLV             ; read all actual voltages
SAVE                 ; save settings to SD card
```

D.3 Running a Pulse Sequence Table

```
STBLDAT;0:[0:1:2:0,500:1:2:50,1000:1:2:0];   ; DC bias ch1: 0→50V at 500µs, return at 1ms
STBLCLK,INT          ; internal clock
STBLTRG,SW           ; software trigger
SMOD,ONCE            ; run once
TBLSTRT              ; fire!
```

D.4 Configuring ARB Twave

```
SARBMODE,1,TWAVE     ; set module 1 to Twave mode
SWFREQ,1,10000       ; 10 kHz
SWFVRNG,1,50         ; 50 Vp-p
SWFTYP,1,SIN         ; sine waveform
SWFDIR,1,FWD         ; forward direction
SWFENA,1             ; start output
```

D.5 Auto-Tuning an RF QUAD

```
SRFATMINF,400000     ; scan from 400 kHz
SRFATMAXF,2000000    ; to 2 MHz
SRFATHP,80           ; Phase 2 drive = 80%
```

```
SRFATSWR,TRUE        ; minimise SWR in Phase 2
SRFATUNER,1          ; auto-tune module 1 with console output
```